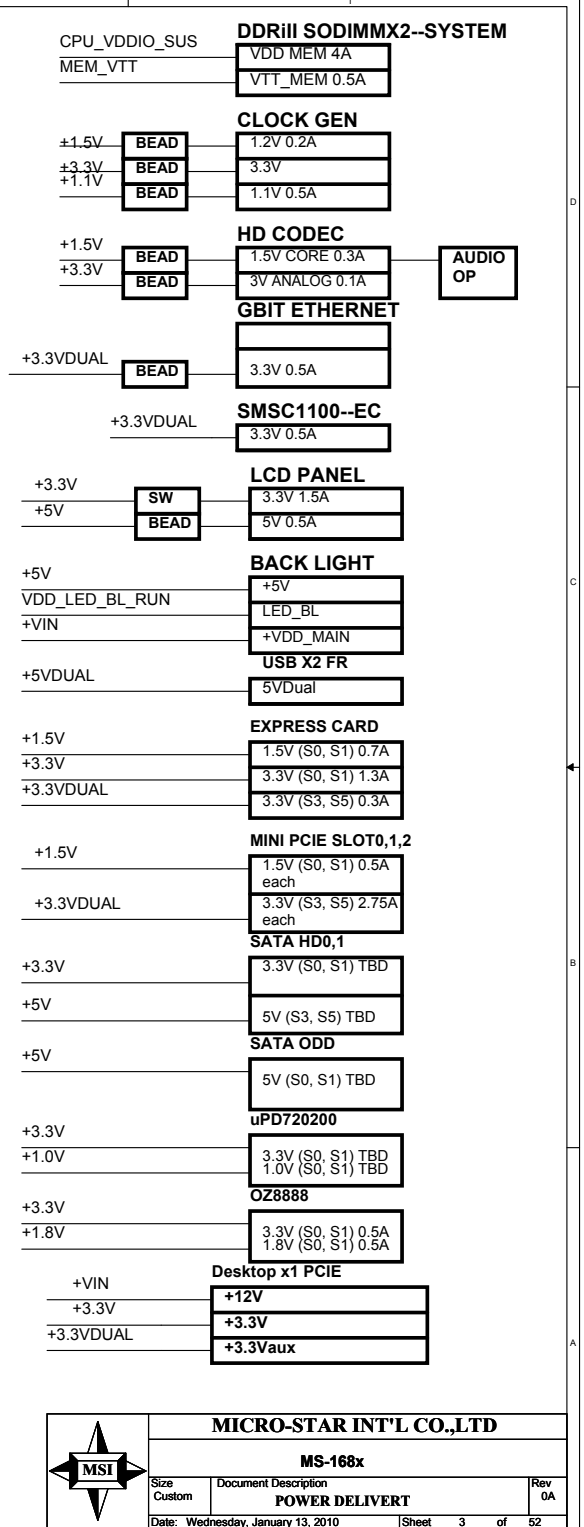
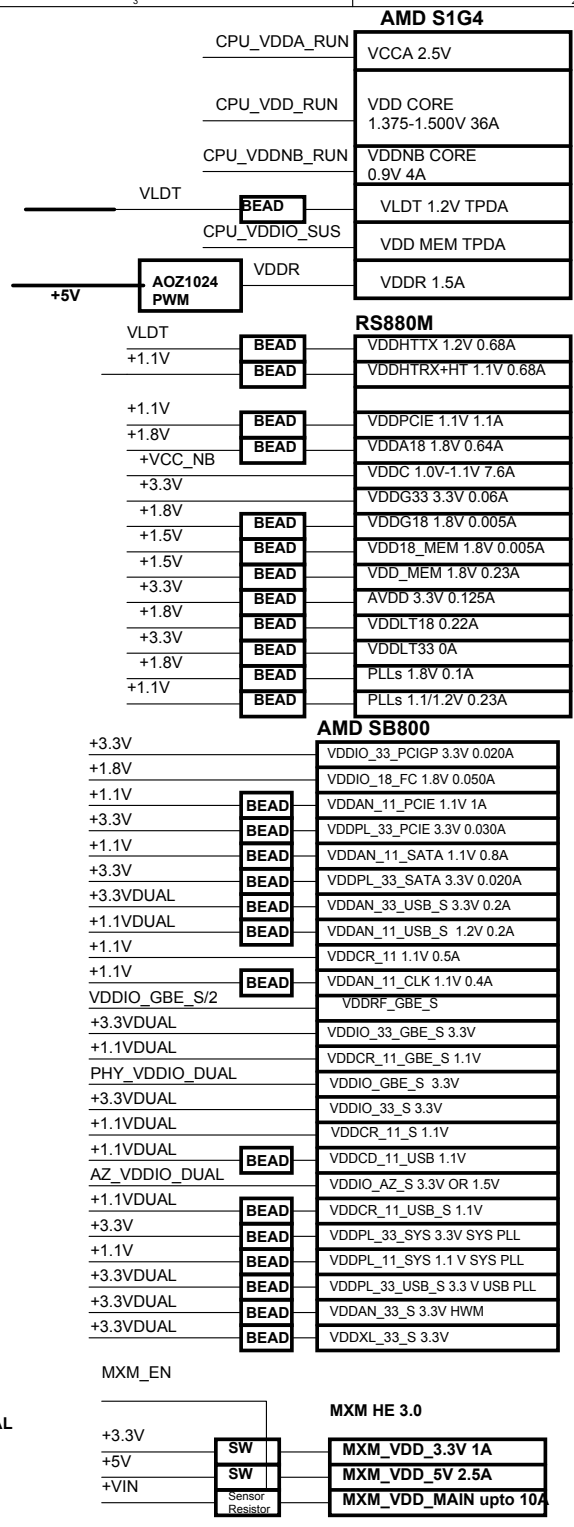
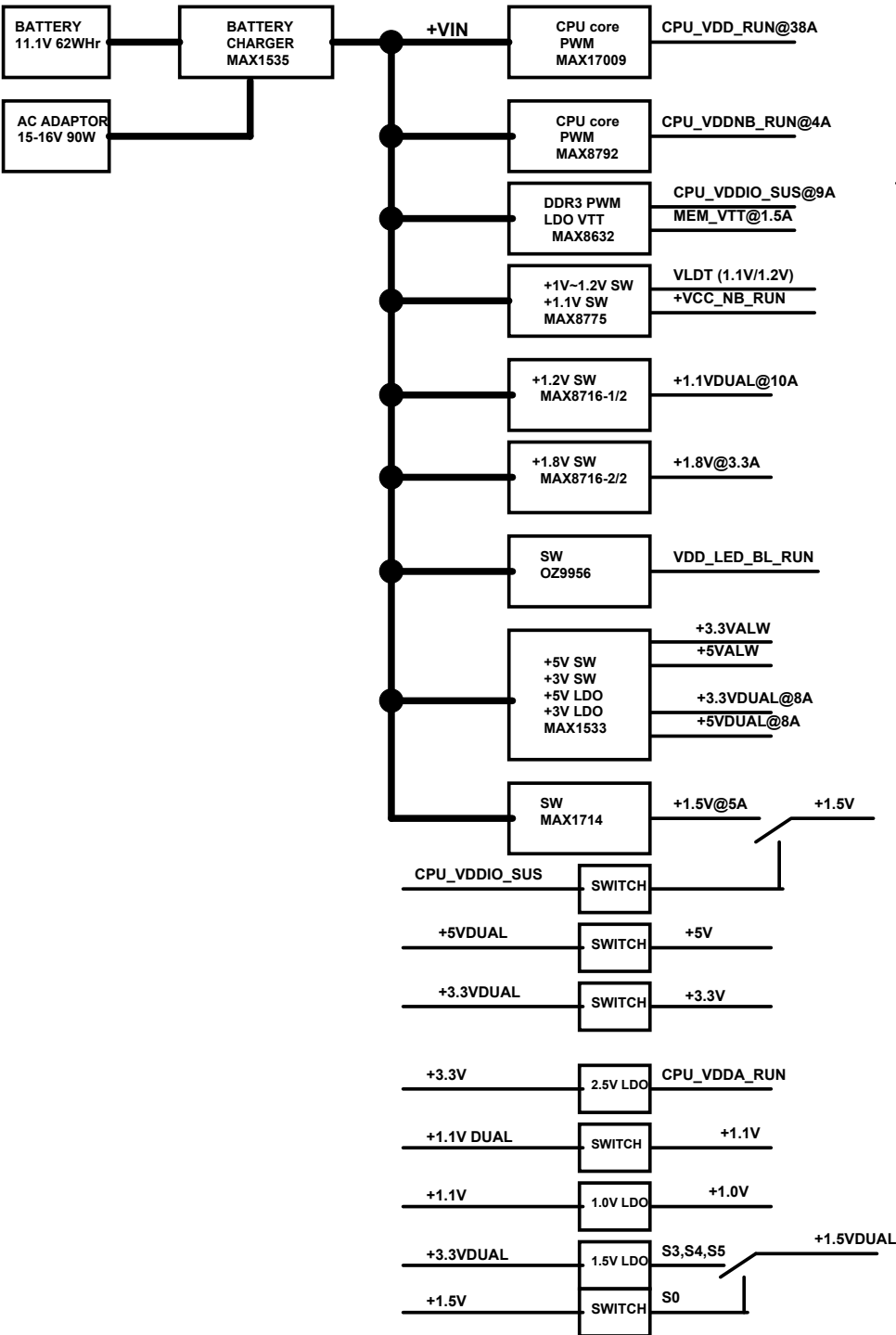


TABLE OF CONTENTS

P01 : BLOCK DIAGRAM	P32 : MXM PWR / MISC
P02 : TABLE OF CONTENTS	P33 : MXM 3.0 EDGE
P03 : POWER DELIVERY CHART	P34 : LVDS / CRT SWITCH
P04 : POWER SEQUENCE CHART	P35 : LVDS CON / BACKLIGHT
P05 : CLOCK DISTRIBUTION	P36 : CRT / LASSO CONN
P06 : MISC TABLES	P37 : EDP / DPD
P07 : BATTERY CHARGER	P38 : DPB / DPC
P08 : CPU CORE PWR	P39 : USB3.0 (1)
P09 : CPU MEM PWR	P40 : USB3.0 (2)
P10 : 1V1DUAL / 1V1 /18V /3V3 /5V	P41 : SATA CONN / DEBUG
P11 : 1V5 / 1V5DUAL	P42 : HD AUDIO CODEC
P12 : NBCORE / VLDT	P43 : HD AUDIO CONN
P13 : SYSTEM POWER	P44 : 1394 / SD READER
P14 : S1G4 HT I/F	P45 : FP / BT / CIR
P15 : S1G4 DDRIII MEMORY I/F	P46 : USB2.0 PORTS
P16 : S1G4 CTRL / DEBUG	P47 : LAN PHY (B50610)
P17 : S1G4 PWR / GND	P48 : MINI PCIE SLOT 0, 3
P18 : DDR3 SODIMMS A/B CHANNLE	P49 : MINI PCIE SLOT 1, 2
P19 : DDR3 SODIMMS DECOUPLING	P50 : X4 GPP / PCIE EXPRESS CARD
P20 : EXTERNAL CLOCK GEN	P51 : LOM (57760)
P21 : RS880M HT I/F	P52 : KBC - SMSC1100L
P22 : RS880M PCIE I/F	P53 : KBCBIOS / KBD /MOUSE
P23 : RS880M SYSTEM	P54 : CONFIG ROM / LPC ROM / TPM
P24 : RS880M SPMEM/STRAPS	P55 : RESET / FAN / LED / PWRGD
P25 : RS880M POWER	P56 : ACPI CONN
P26 : SB8X0 PCIE/PCI/CPU/LPC/CLK	P57 : DEBUG - POST LEDS
P27 : SB8X0 GPIO/USB/AZ/RGMII	P58 : DUAL RAIL ENABLE
P28 : SB8X0 SATA/IDE/HWM/SPI	P59 : DISCHARGE CIRCUIT
P29 : SB8X0 POWER / DECOUPLING	P60 : SB800 A11 PU RES
P30 : SB8X0 STRAPS	P61 : CHANGE HISTROY
P31 : PCIE SWITCH	P62 : POWER ON SEQUENCE CHART



Power on Sequence required:

SB800:
1, +3.3VDUAL ramp before +1.1VDUAL
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3, +1.1V ramp before VCC_NB

SB OUTPUT
--NB_PWRGD
NB_PWRGD_IN
SB INPUT
--SB_PWRGD

GROUP B

GROUP A


CPU MEM CTL & DDR3 SODIMM PWRs

**CPU_THM/SB/SCL1/2
SB_KB/SPI/LPC ROM PWRs**

KBC is ready

**KBC is powered by
A_VBAT & +3.3VALW**

A_VBAT



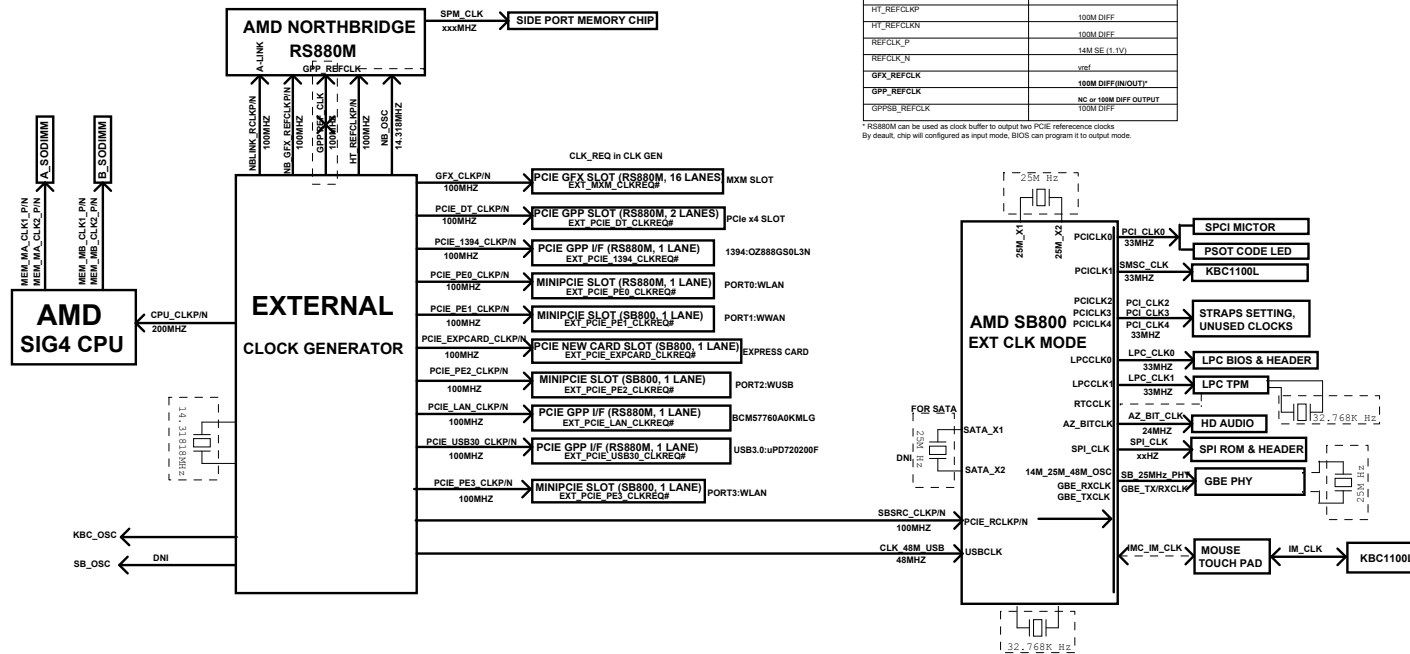
MICRO-STAR INT'L CO.,LTD

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Size Custom Document Description **POWER SEQUENCE** Rev GA

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EXTERNAL CLOCK MODE

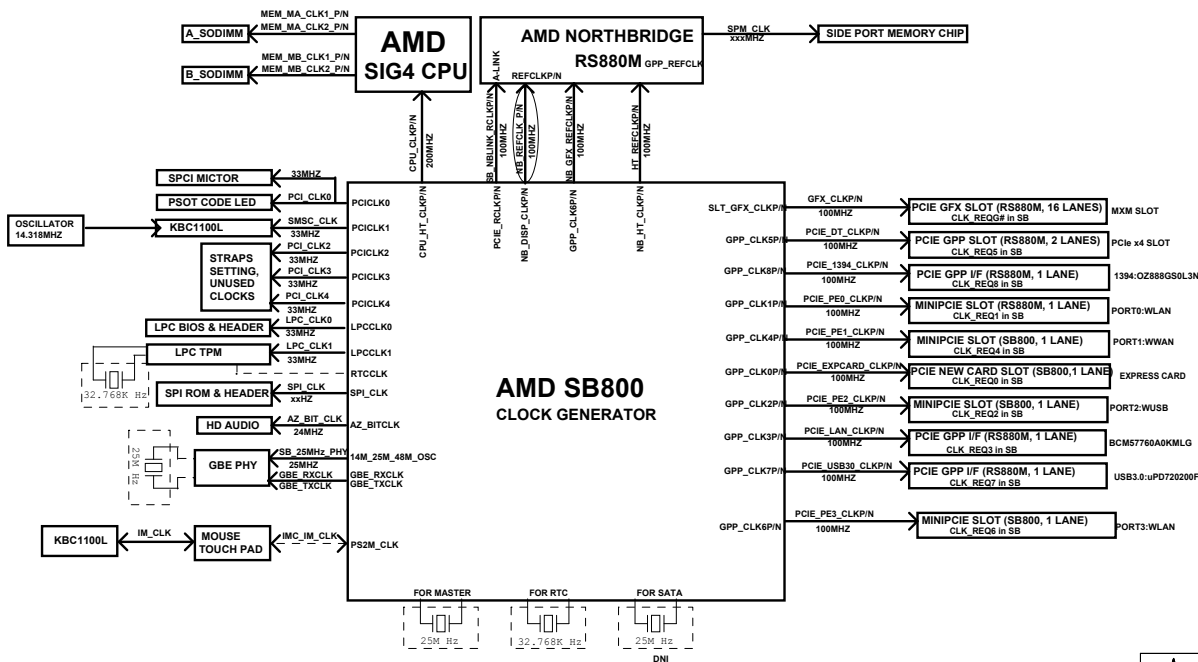


NB CLOCK INPUT TABLE

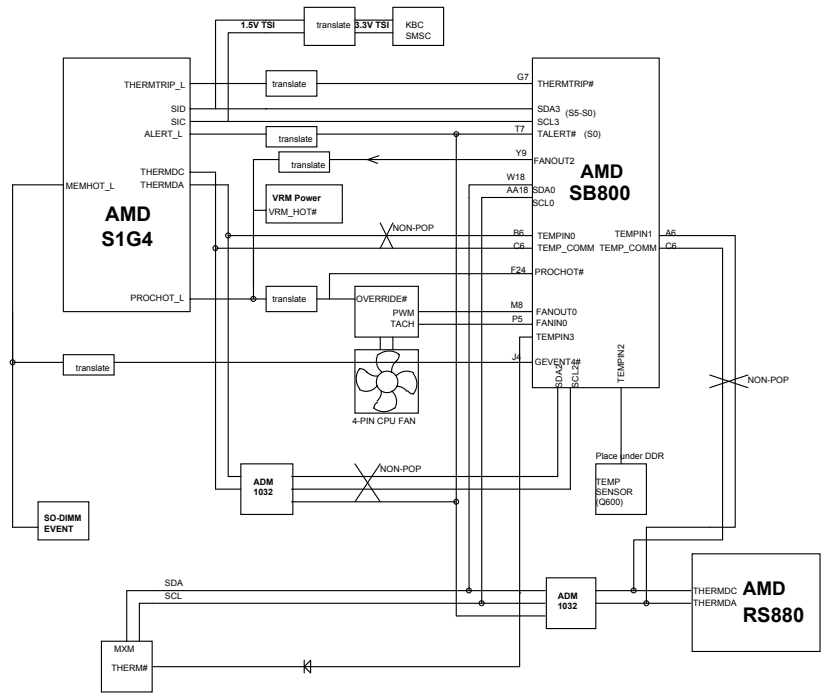
NB CLOCKS	RS880M
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1 TV)
REFCLK_N	14M SE (1 TV)
GFX_REFCLK	100M DIFF/INOUT
GPP_REFCLK	100M DIFF/INOUT
GPPB_REFCLK	100M DIFF

* RS880M can be used as clock buffer to output two PCIe reference clocks
By default, chip will configured as input mode, BIOS can program it to output mode.

INTERNAL CLOCK MODE



Thermal Systems
(Emergency Shutdown, Throttling, Fan Control)

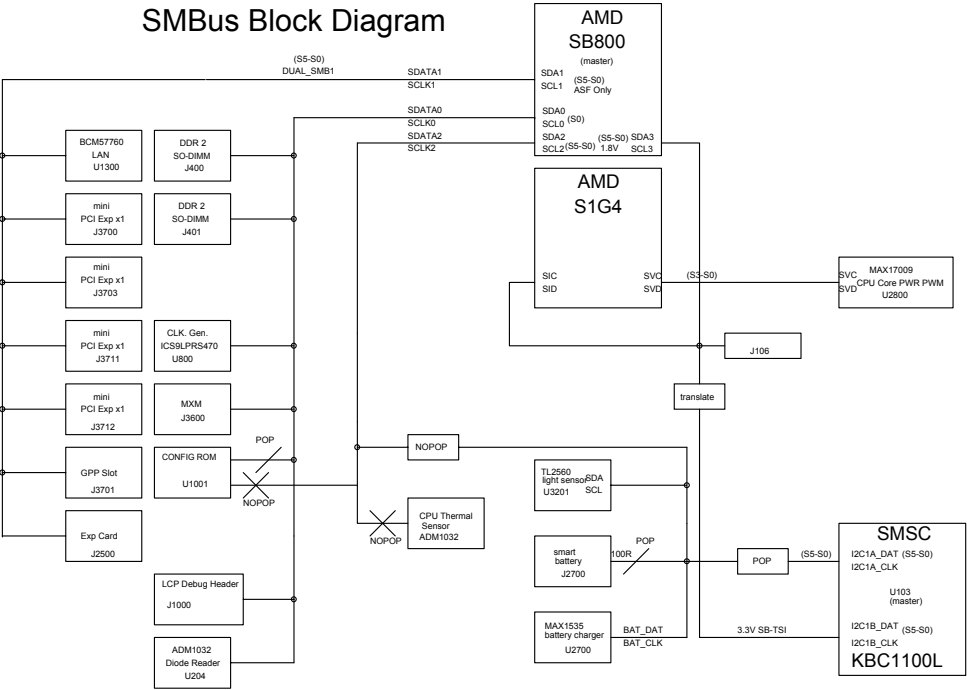


Thermal disaster prevention is implemented by PROCHOT_L and THERMTRIP_L with hardware non-system dependant functions. Fan speed control will only be implemented by SB TSI software based implementation

Power State / Voltage Rail Activity Summary

Global System State	Sleep State	Processor Power State	Description	RTC	ALW	DUAL	SUS	RUN
G0	S0	C0	Running	ON	ON	ON	ON	ON
G0	S0	C0	Running	P-state transitions under OS control	ON	ON	ON	ON
G0	S0	C1	Halt	ON	ON	ON	ON	ON
G0	S0	C2	Stop grant, caches snooperable	ON	ON	ON	ON	ON
G0	S0	C3	TBD	ON	ON	ON	ON	ON
G0	S0	c4	TBD	ON	ON	ON	ON	ON
G1	S1	OFF	Powered on suspend	ON	ON	ON	ON	ON
G1	S3	OFF	Suspend to RAM	ON	ON	ON	ON	OFF
G2	S4	OFF	Suspend to disk	ON	ON	ON	OFF	OFF
G2	S5	OFF	Soft-off	ON	ON	ON	OFF	OFF
G2/G3	S5 LOW	OFF	Battery IN	ON	ON	ON	OFF	OFF
G3	OFF	OFF	Mechanical off	ON	OFF	OFF	OFF	OFF

SMBus Block Diagram



Group Name Description

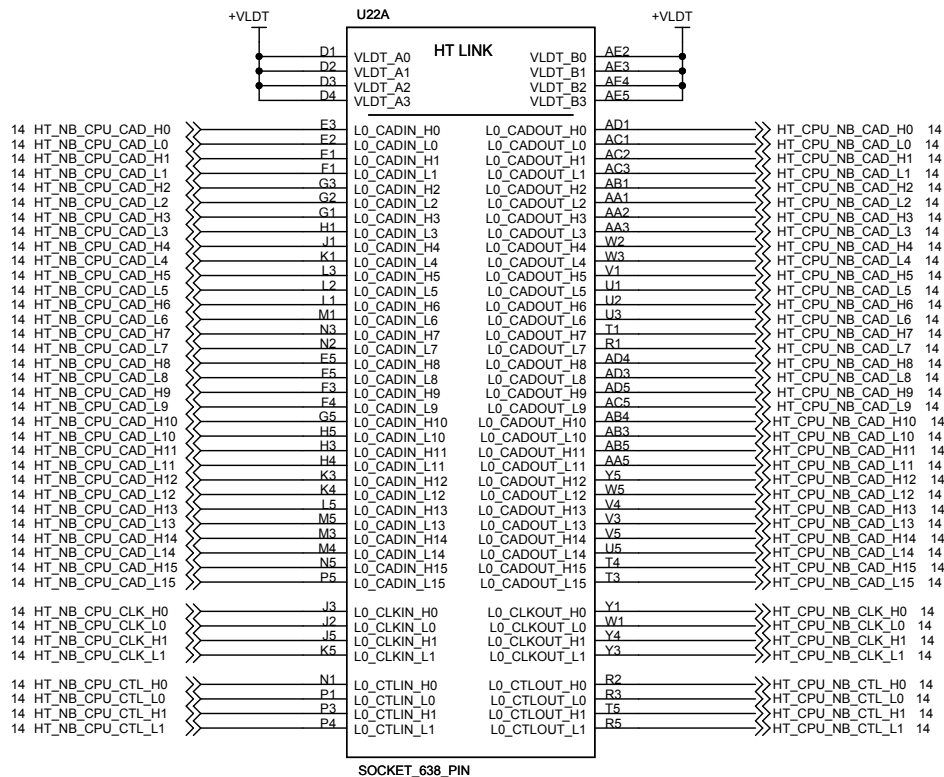
INT: Stuff when use internal clock generator
EXT: Stuff when use external clock generator
DNI: DO NOT INSTALL
KBC: Stuff when use external KBC
IMC: Stuff when use internal EC
A11:Resistors marked with "A11" is only for SB800A11 ONLY.

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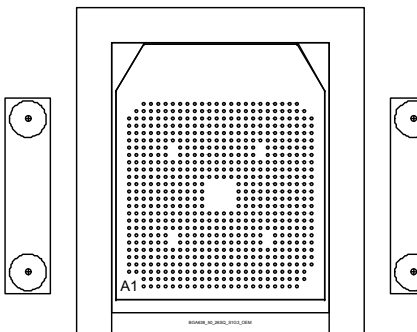
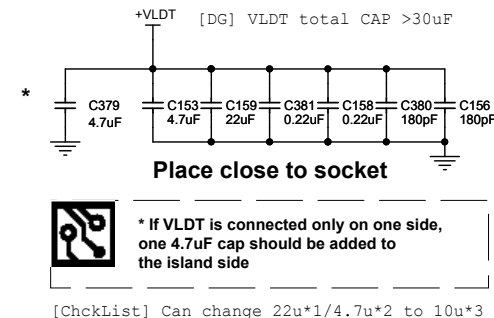
Size CustomDocument DescriptionSMBUS BLOCKRev 0A

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SOCKET_638_PIN

[CheckList] If the I/O device does not support the CTLIN1 pair, pull up 51ohm

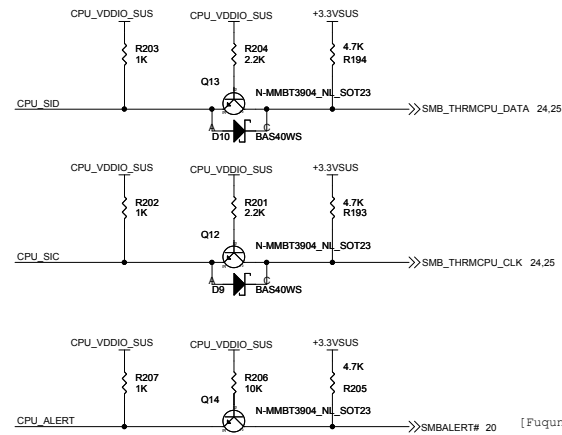
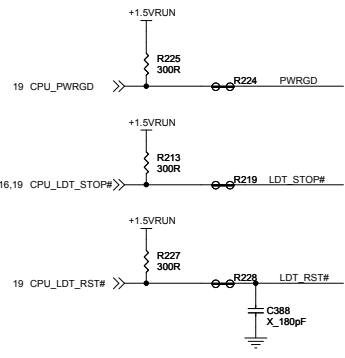


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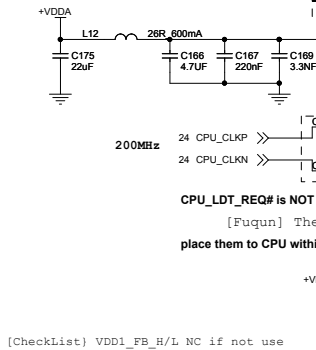
Size B	Document Description	Rev 0A
	SIG4 HT I/F	
Date: Friday, February 05, 2010	Sheet 7 of 52	

Keep net PWRGD, LDT_STOP#, LDT_RST# no stub



THERMDA/THERMDC is not used;
CPU thermal control is based on TSI by default.

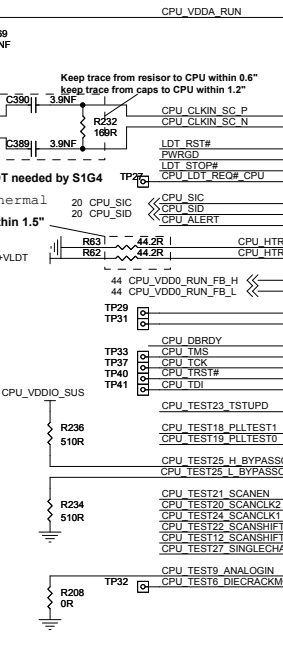
[DG] BEAD: R<40mΩ (about 35), I>500mA
[ChckList] VDDA:100u*1/4.7u*1/0.22u0603*1/3300p0603*1



[CheckList] VDDI_FB_H/L NC if not use



LAYOUT: ROUTE VDDA TRACE APPROX
50 mils WIDE (USE 2x25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.



[Fuqun] RSVD/TEST6/7/8/10/28--NC

[Fuqun] TEST14/15/16/17--Test Point

[Fuqun] TEST23/25--Test Point

[Fuqun] TEST12/18-24--Pull down 1Kohn to VSS

[Fuqun] TEST27 pull-up 1Kohm to VDDIO

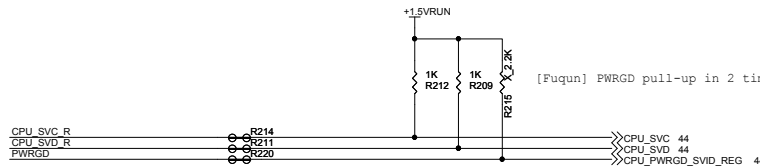
[Fuqun] TEST25_H pull-up 510ohm to VDDIO

[Fuqun] TEST25_L pull-down 510ohm to VSS

[Fuqun] TEST9 is tied to VSS

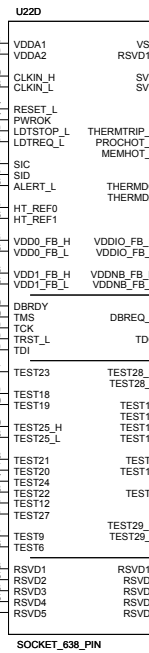
[Fuqun] There is a (±1%) differential termination between TEST29_L and TEST29_H

[Fuqun] CPU_DBRDY not need pull down in checklist



SVC	SVD	BOOT VOLTAGE(VDD)	
		(CPUVRN_PROG = VCC30N)	(CPUVRN_PROG = OPEN)
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

VID OVERRIDE TABLE (VDD)



SOCKET_638_PIN

[Fuqun] TEST23--R358 NC in ref schematic?

[Fuqun] PWRGD pull-up in 2 times (R187 and R163)?

[Fuqun] PWRGD pull-up in 2 times (R187 and R163)?

[DateSheet] Internal pull up 870-1250 ohm:
SSA[2:0], TCK, TMS, TRST_L, TDI, DBREQ_L, PLATFORM_TYPE, TEST27

[DateSheet] Internal pull down 870-1250 ohm:
TEST12, TEST[20:24]

Internal pull up 870-1250 ohm:
SSA[2:0], TCK, TMS, TRST_L, TDI, DBREQ_L, PLATFORM_TYPE, TEST27

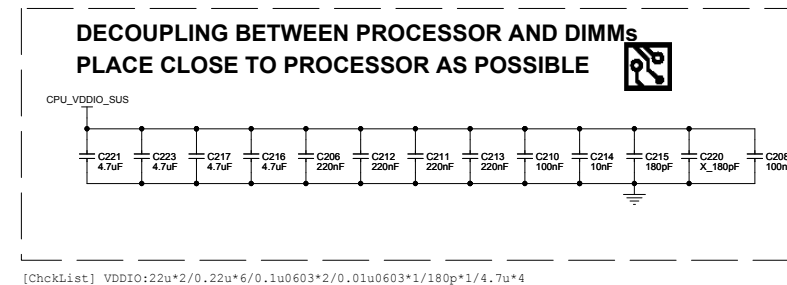
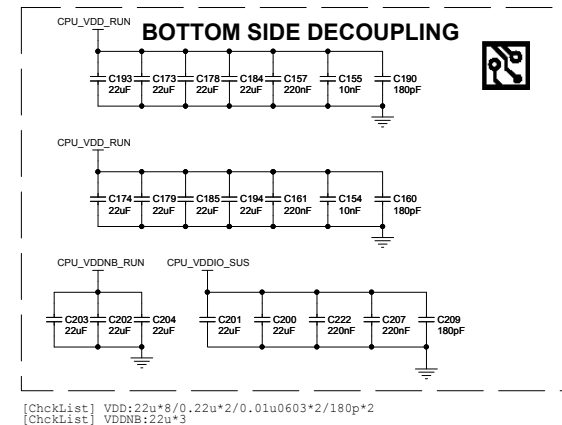
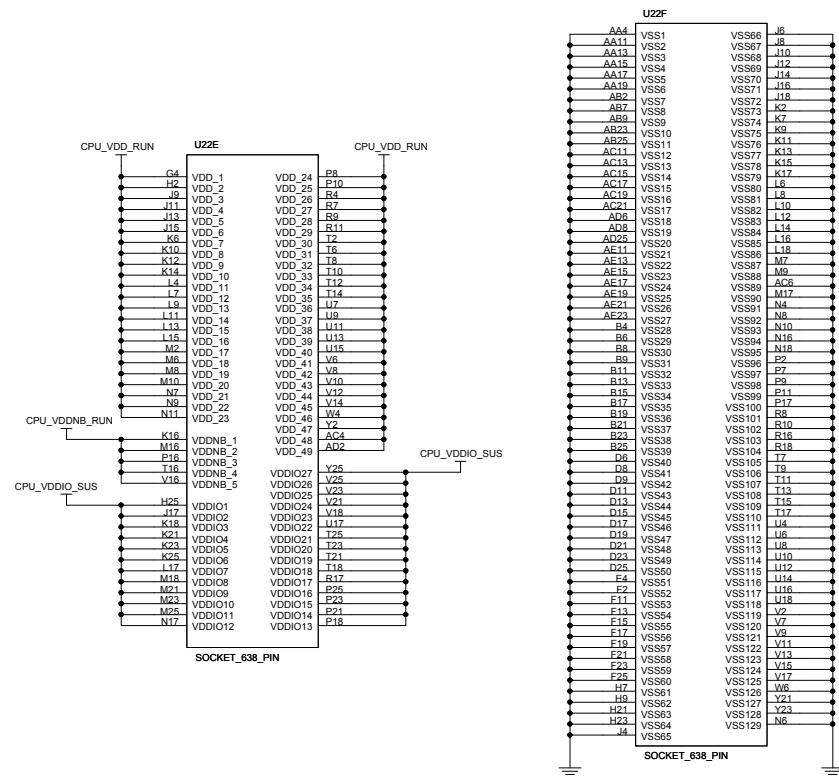


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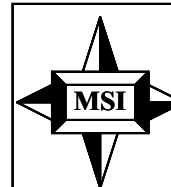
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PROCESSOR POWER AND GROUND



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Custom	SIG4 POWER and GND	0A	
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MICRO-STAR INT'L CO.,LTD

MS-168xSize
A

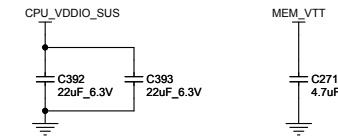
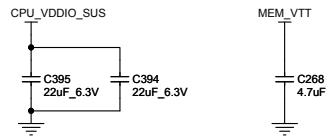
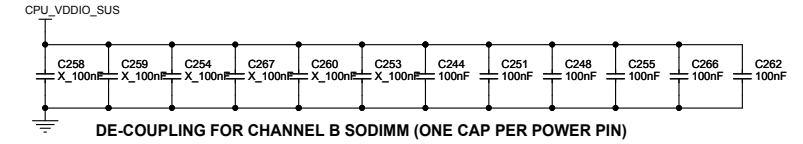
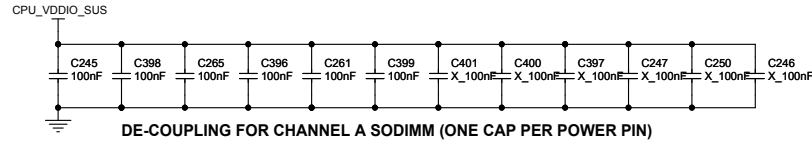
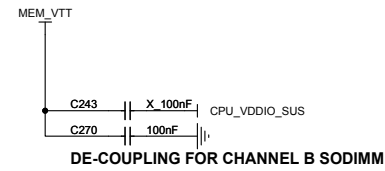
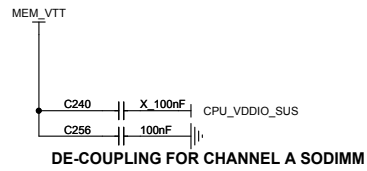
Document Description

DDR3 SO-DIMM-B

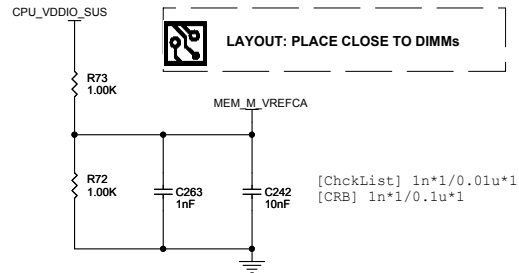
Rev	0A
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Date: Wednesday, January 13, 2010

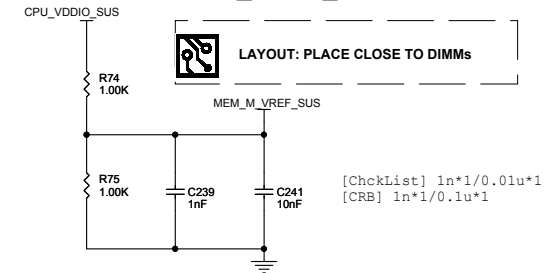
Sheet 12 of 52



MEM_M_VREFCA



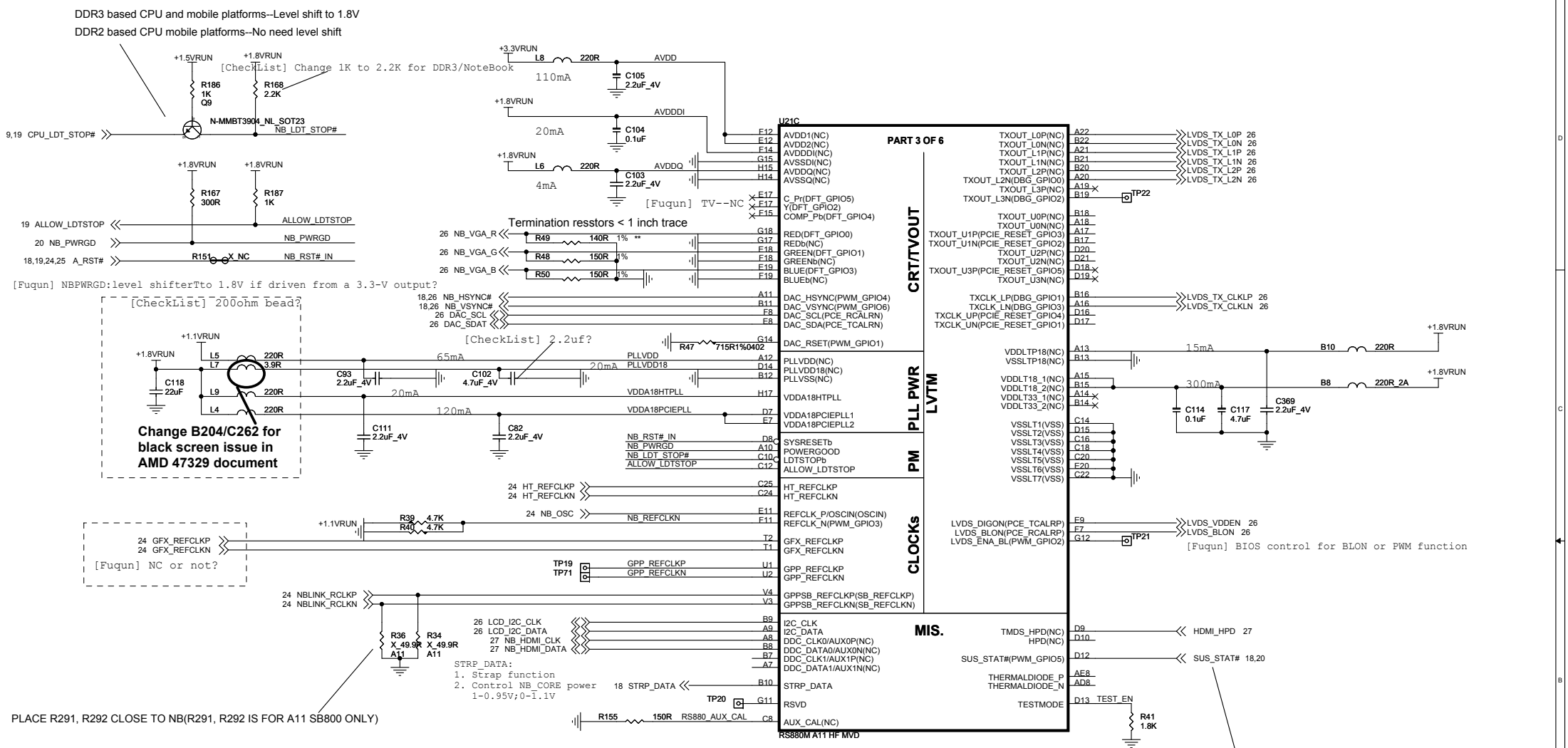
MEM_VREF_SUS



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Custom	DDR3 DECOUPLING	0A
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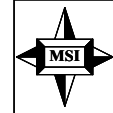


PLACE R291, R292 CLOSE TO NB(R291, R292 IS FOR A11 SB800 ONLY)

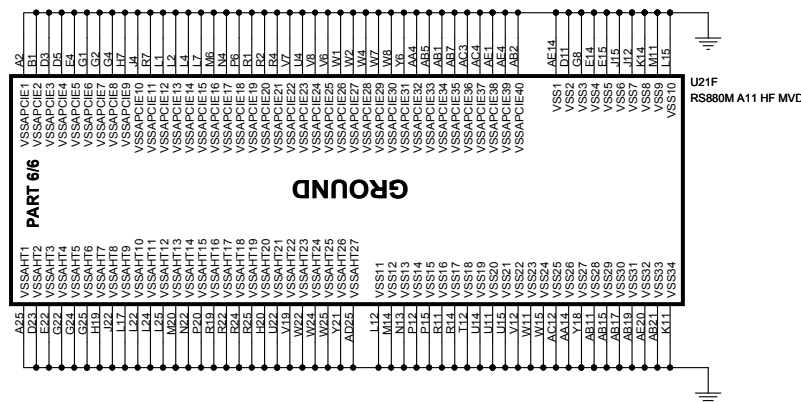
[Fuqun] SUS_STAT#-->Not need connect to SB if Side-Port memory not implemented

RS880M DEBUG PIN MAPPING

DEBUG_OUT0	LVDS_DIGON
DEBUG_OUT1	LVDS_ENA_BL
DEBUG_OUT2	LVDS_BLOW
DEBUG_OUT3	TMDS_HPD
DEBUG_OUT4	AUX1N
DEBUG_OUT5	AUX1P
DEBUG_OUT6	HPD
DEBUG_OUT7	AUX_CAL



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RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD0	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD0	+1.1V
VDD18_MEM	+1.8V	PLLVD018	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVD018	+1.8V	VDDLT33	NC

[CheckList] VDDHT can share with VDDC

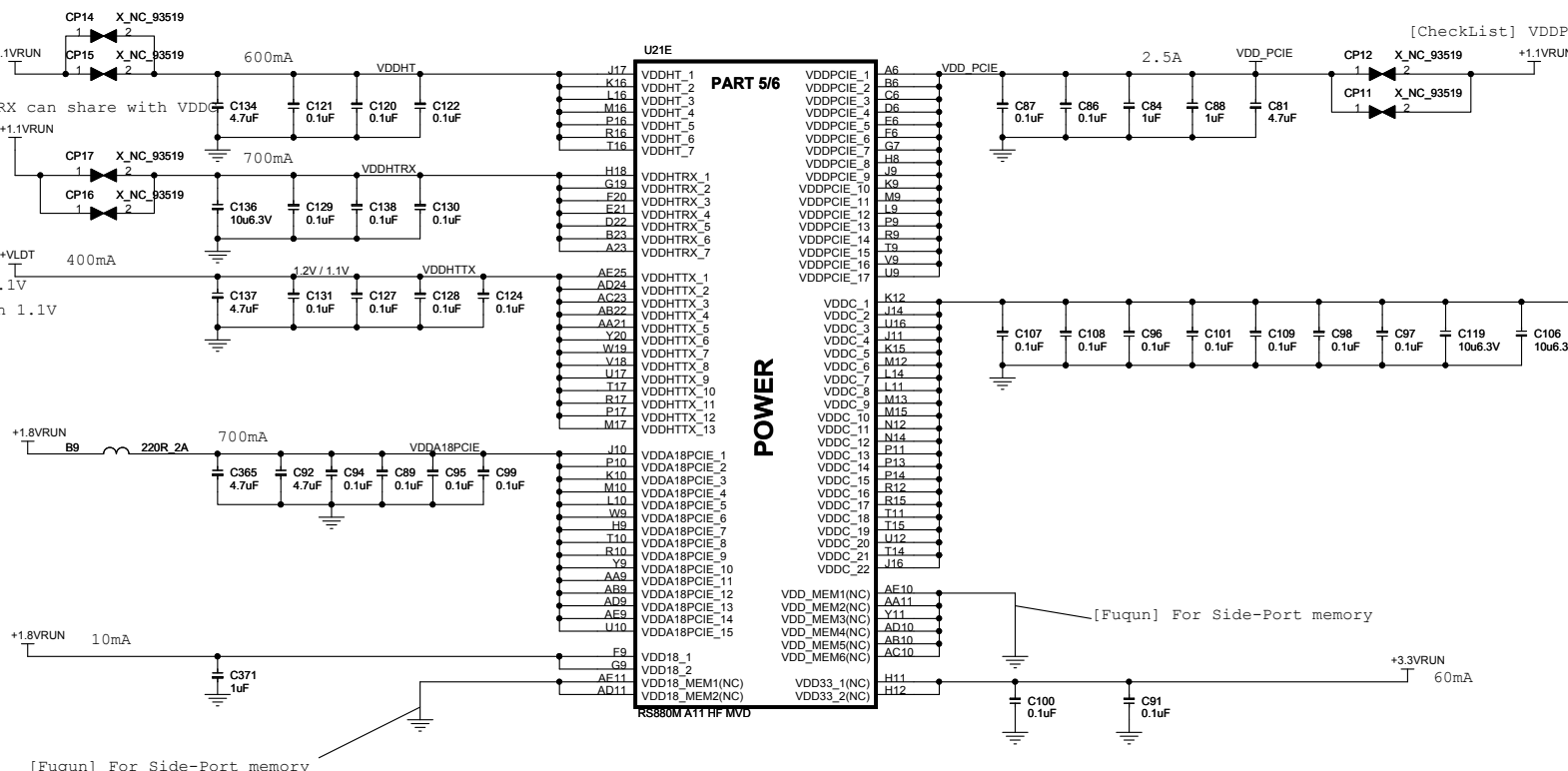
[CheckList] VDDHTRX can share with VDDC

[Fuqun] 1.2V or 1.1V

[Fuqun] Share with 1.1V

[CheckList] VDDPCIE can share with VDDC

[CheckList] 0.95V~1.1V 10A
10u*2/0.1u*7



[Fuqun] For Side-Port memory

[Fuqun] For Side-Port memory



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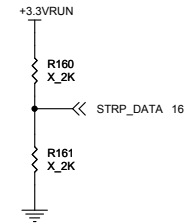
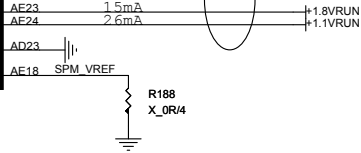
Size	Document Description	Rev
Custom	RS880M-POWER	0A
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U21D		
PAR 4 OF 6		
AB12	MEM_A0(NC)	MEM_DQ0/DVO_VSYNC(NC)
AE16	MEM_A1(NC)	MEM_DQ1/DVO_HSYNC(NC)
V11	MEM_A2(NC)	MEM_DQ2/DVO_DE(NC)
AE15	MEM_A3(NC)	MEM_DQ3/DVO_D0(NC)
AD12	MEM_A4(NC)	MEM_DQ4(NC)
AB16	MEM_A5(NC)	MEM_DQ5/DVO_D1(NC)
AD14	MEM_A6(NC)	MEM_DQ6/DVO_D2(NC)
AD13	MEM_A7(NC)	MEM_DQ7/DVO_D4(NC)
AD15	MEM_A8(NC)	MEM_DQ8/DVO_D3(NC)
AC16	MEM_A9(NC)	MEM_DQ9/DVO_D5(NC)
AE13	MEM_A10(NC)	MEM_DQ10/DVO_D6(NC)
AC14	MEM_A11(NC)	MEM_DQ11/DVO_D7(NC)
Y14	MEM_A12(NC)	MEM_DQ12(NC)
	MEM_A13(NC)	MEM_DQ13/DVO_D9(NC)
AD16	MEM_BA0(NC)	MEM_DQ14/DVO_D10(NC)
AE17	MEM_BA1(NC)	MEM_DQ15/DVO_D11(NC)
AD17	MEM_BA2(NC)	
	MEM_DQS0P/DVO_IDCKP(NC)	
	MEM_DQS0N/DVO_IDCKN(NC)	
W12C	MEM_RASb(NC)	MEM_DQS1P(NC)
Y12C	MEM_CASb(NC)	MEM_DQS1N(NC)
AD18C	MEM_WEb(NC)	
AB13C	MEM_CSb(NC)	
AB18	MEM_CKE(NC)	MEM_DM0(NC)
Y14	MEM_ODT(NC)	MEM_DM1/DVO_D8(NC)
V15	MEM_CKP(NC)	IOPLLVD18(NC)
W14	MEM_CKN(NC)	IOPLLVD1(NC)
AE12	MEM_COMP(NC)	IOPLLVS(NC)
AD12	MEM_COMPN(NC)	MEM_VREF(NC)

SBD_MEM/DVO_I/F

RS880M A11 HF MVD

[Fuqun] Remove Bead and Cap follow CheckList



NOTE: Providing access to STRAP_DATA and I2C_CLK pins is MANDATORY.

[Fuqun] STRP_DATA pull down in Ref-schematic

STRAP_DEBUG_BUS_GPIO_ENABLEb

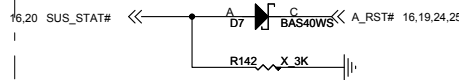
Enables the Test Debug Bus using GPIO.

RS880M	
1 Disable	
0 Enable	

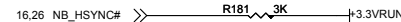
DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected



[Fuqun] SUS_STAT# pull up in SB side



RS880M: Enables Side port memory

RS880M:HSYNC#

Selects if Memory SIDE PORT is available or not

1 = Memory Side port Not available

0 = Memory Side port available

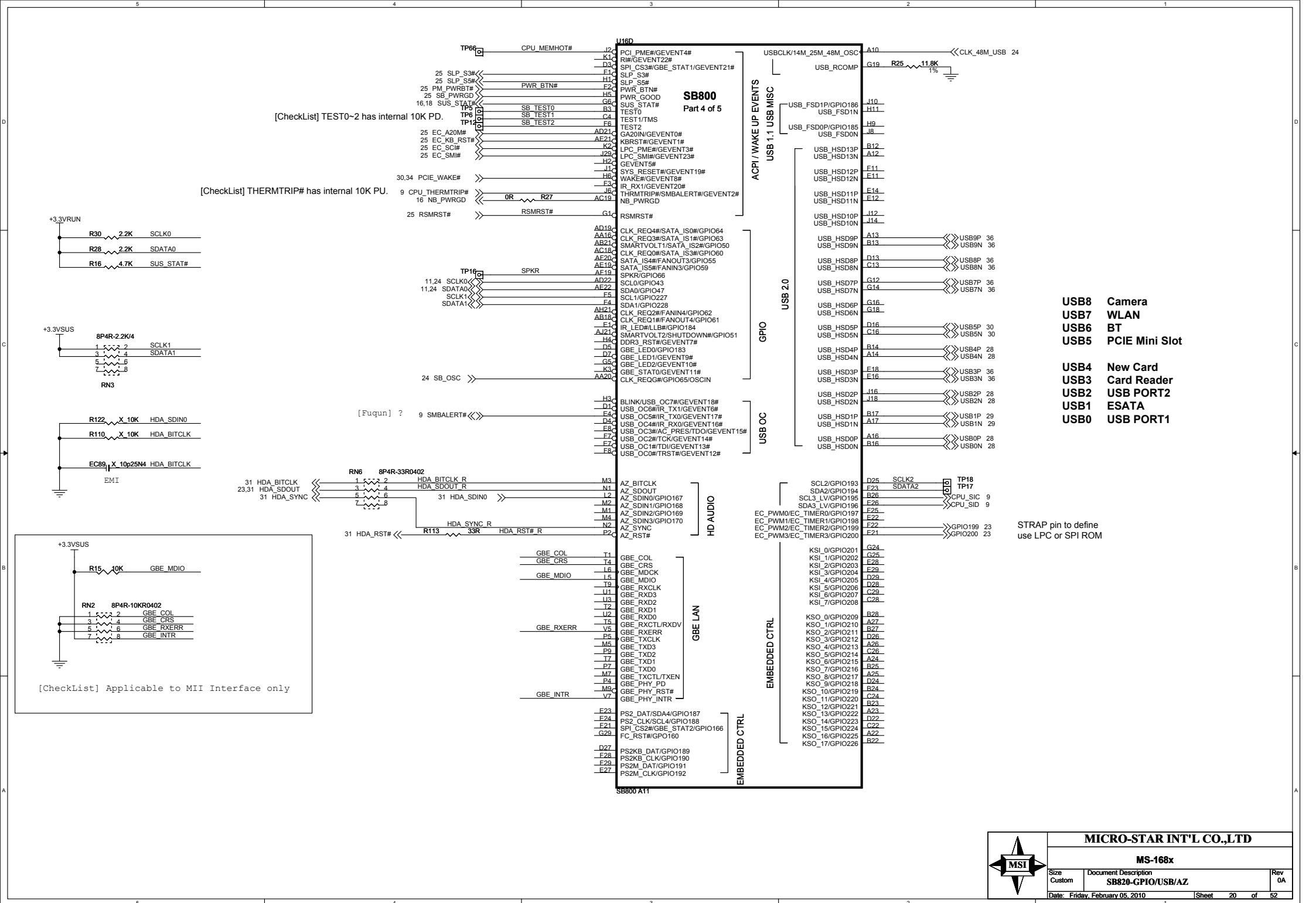
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]



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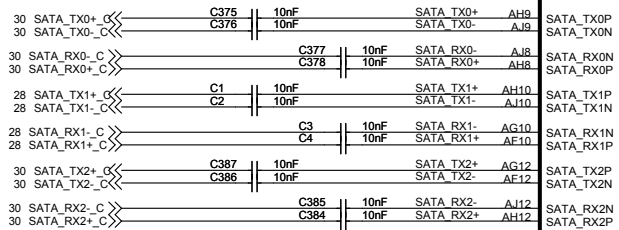
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SATA trace should use only 1via on the trace.
customers can use 2vias with GND via within 150mils of
signal via as long as they can ensure that their platform
meets SATA logo requirements. Return loss is expected
to get affected with 2 vias. AMD platforms are validated
with one via only

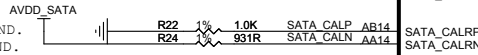


SATA PORTS DISTRIBUTION:
0, - 2.5 INCH DISK DRIVER
1, SATA ODD
2, - 2.5 INCH DISK DRIVER
3, eSATA
4 & 5, NOT USED

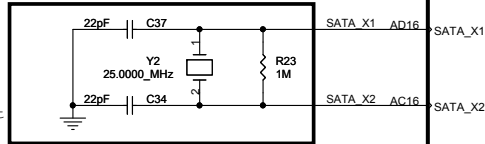


PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF U600

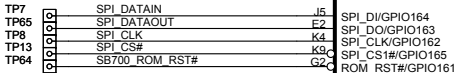
SATA_CALRP:
SB8xx A11: 800-? 1% resistor to GND.
SB8xx A12: 1K-? 1% resistor to GND.



To meet SB800 SCL1.02:
DNI SATA XTAL circuit's parts



[Fuqun] Not installed by default



Jameslee: Don't share BIOS and EC rom.

U16B

SB800 Part 2 of 5

SERIAL ATA

HW MONITOR

SPI ROM

FLASH

FC_CLK# AH28
FC_FBCLKOUT# AG28
FC_FBCLKIN# AE26
FC_OE#/GPIO145 AE28
FC_AVD#/GPIO146 AG28
FC_WE#/GPIO148 AE27
FC_CE1#/GPIO149 AE29
FC_CE2#/GPIO150 AE29
FC_INT1/GPIO144 AE29
FC_INT2/GPIO147 AH27
FC_ADQ0/GPIO128 AJ27
FC_ADQ1/GPIO129 AJ26
FC_ADQ2/GPIO130 AH25
FC_ADQ3/GPIO131 AJ24
FC_ADQ4/GPIO132 AG23
FC_ADQ5/GPIO133 AH23
FC_ADQ6/GPIO134 AJ22
FC_ADQ7/GPIO135 AG21
FC_ADQ8/GPIO136 AH22
FC_ADQ9/GPIO137 AJ23
FC_ADQ10/GPIO138 AE23
FC_ADQ11/GPIO139 AJ24
FC_ADQ12/GPIO140 AJ24
FC_ADQ13/GPIO141 AJ25
FC_ADQ14/GPIO142 AG25
FC_ADQ15/GPIO143 AH26

FANOUT0/GPIO52 W5
FANOUT1/GPIO53 W6
FANOUT2/GPIO54 Y9
FANIN0/GPIO56 W7
FANIN1/GPIO57 V9
FANIN2/GPIO58 W8

TEMPIN0/GPIO171 B6
TEMPIN1/GPIO172 AG
TEMPIN2/GPIO173 AG
TEMPIN3/TALERT#/GPIO174 B6
TEMP_COMM C7

VINO/GPIO175 A3
VIN1/GPIO176 B4
VIN2/GPIO177 A4
VIN3/GPIO178 C5
VIN4/GPIO179 A7
VIN5/GPIO180 B7
VIN6/GBE_STAT3/GPIO181 B8
VIN7/GBE_LED3/GPIO182 A8

NC1 G27
NC2 Y2

Connect C7 and D8, then go to GND directly.

[Fuqun] HWM need pull-low follow MS-124X?



NOTE: ROUTE TEMP_COMM
AS A 10MIL TRACE



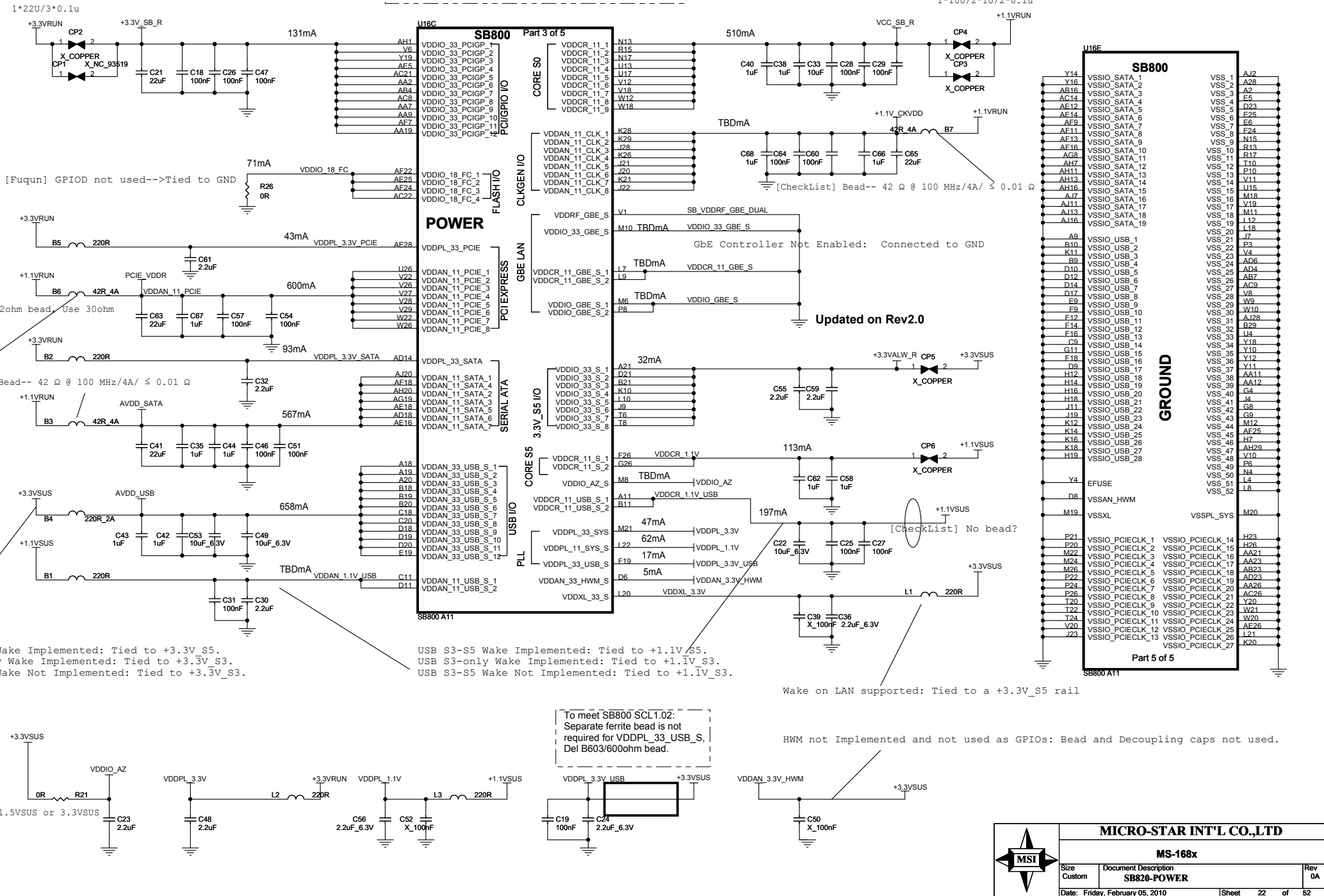
MICRO-STAR INT'L CO.,LTD

MS-168x

Size	Document Description	Rev
Custom	SB820-SATA/IDE/SPI/HWM	0A
Date: Friday, February 05, 2010		Sheet 21 of 52



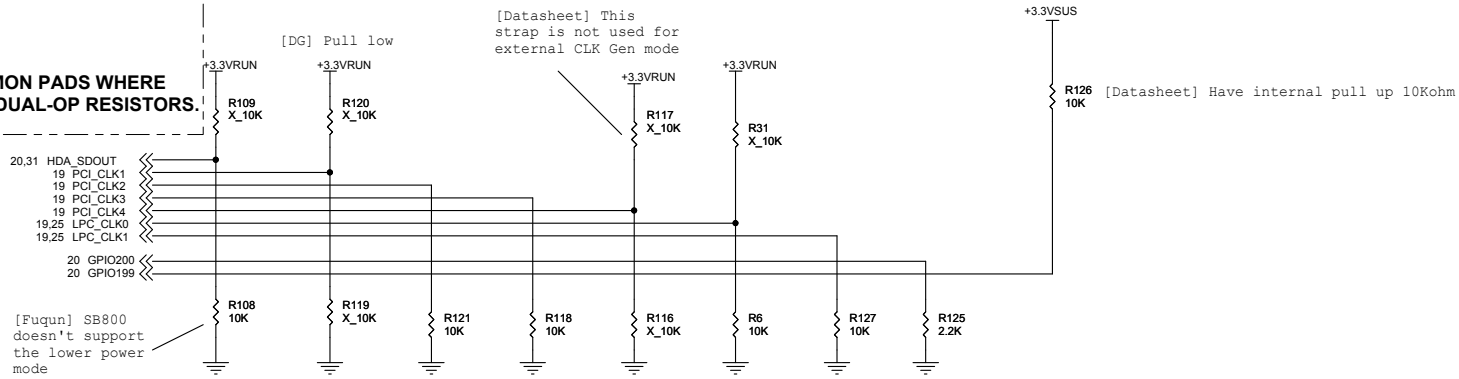
PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.



MICRO-STAR INT'L CO.,LTD			
MS-168x			
Size Custom	Document Description SB820-POWER	Rev 0A	
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OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default)	L,L = FWH ROM

PCI_CLK1(SMSC_CLK)-->SB820M: Only provision for pull-down is required, not installed by default--checklist

[Fuqun] GPIO199 NC in checklist

[Fuqun] PCI_CLK4 high or low?

SB PCIE EEPROM STRAPS

19 CLKREQ5#_GPIO42

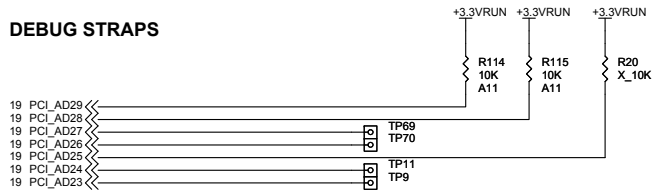
19 CLKREQ7#_GPIO46

TP15

TP14

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

PCI23/24/26/27 have internal pull high 15kohm, But PCI25?

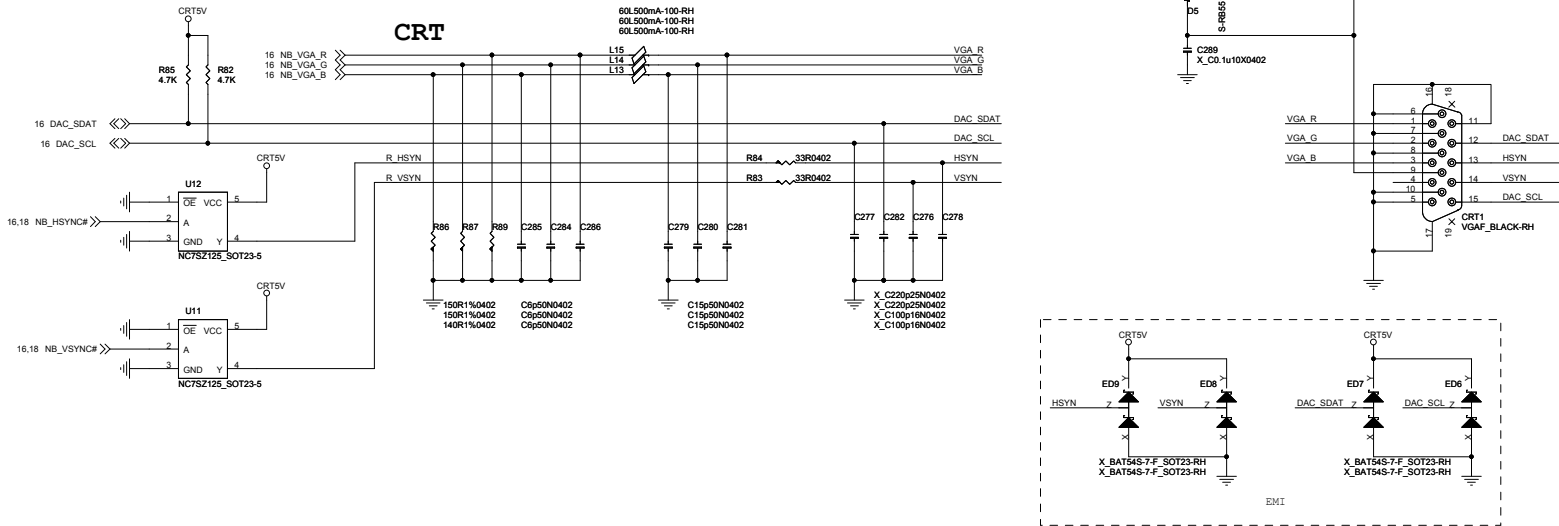
Why PCI28/29 pull high?



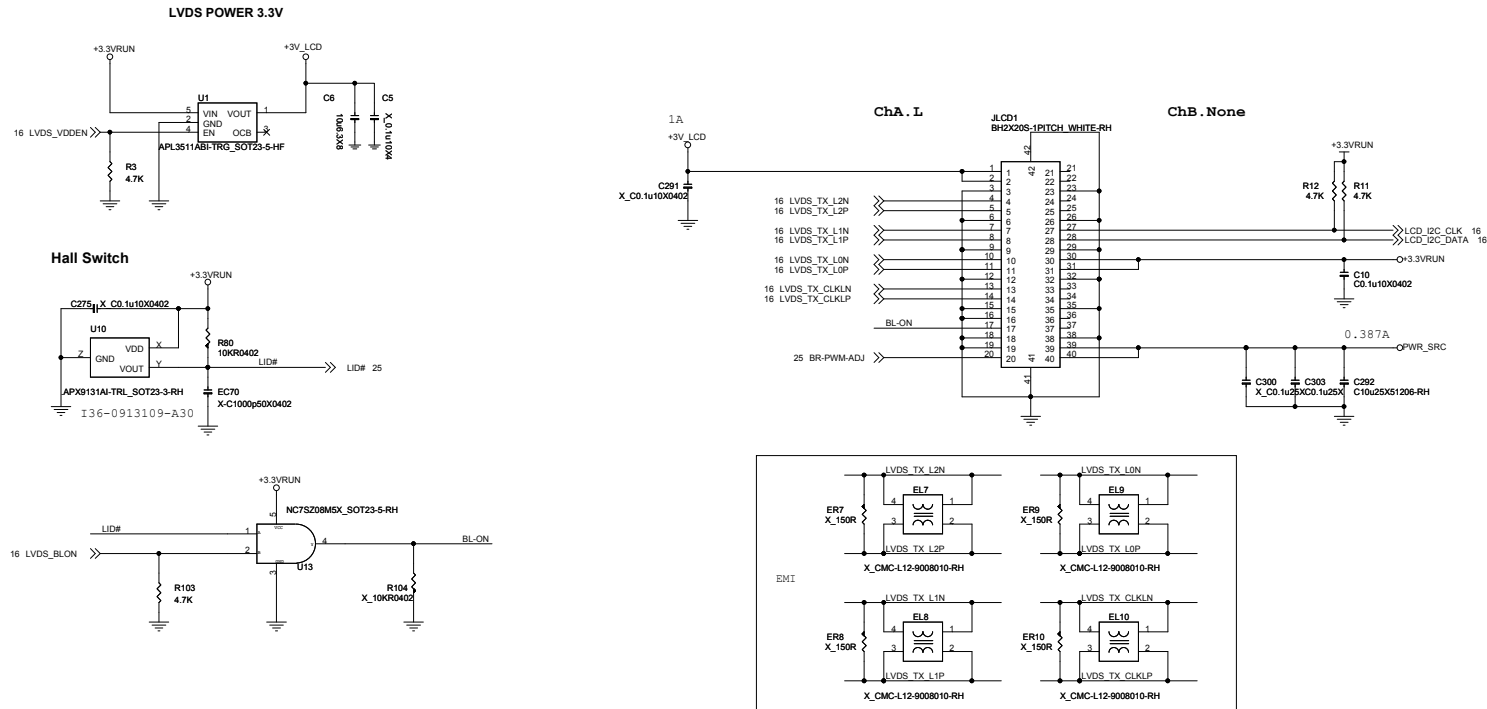
MICRO-STAR INT'L CO.,LTD

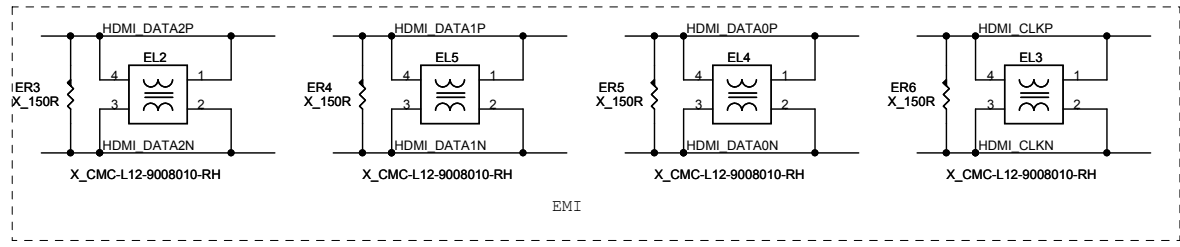
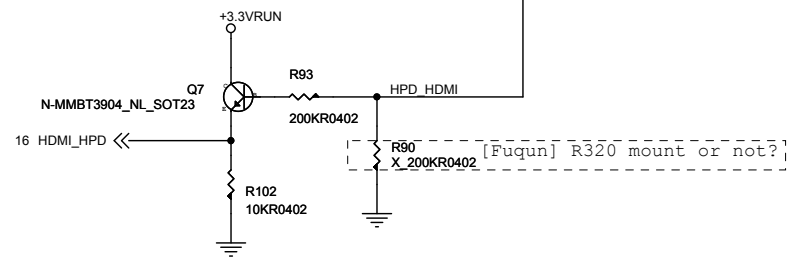
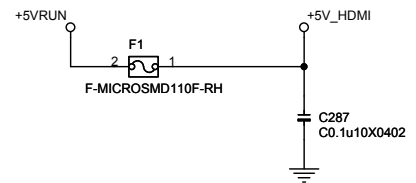
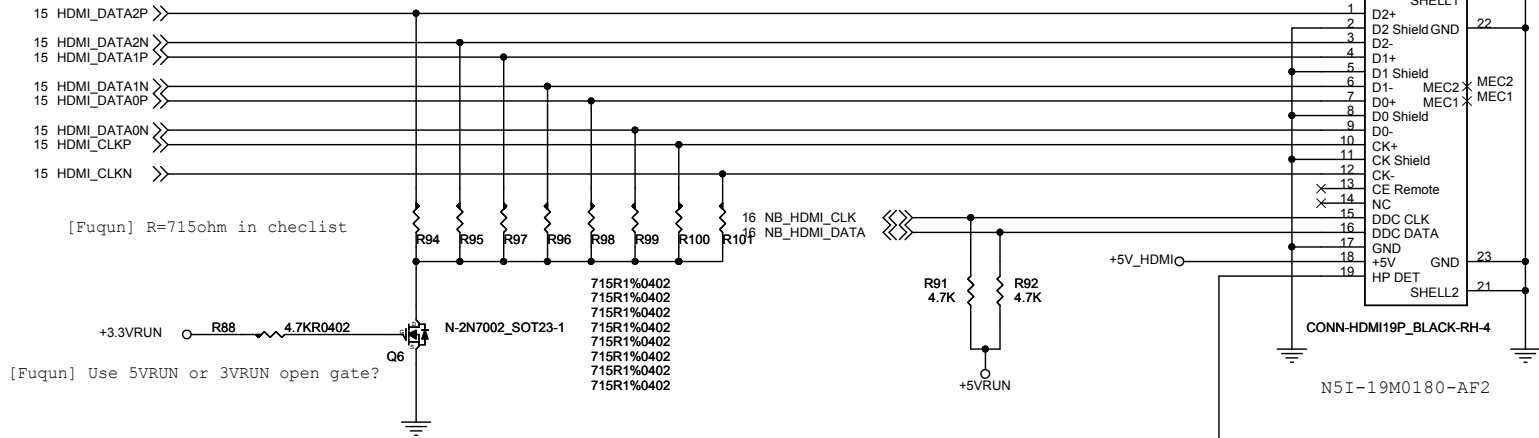
MS-168x

Size Custom	Document Description SB820-STRAPS	Rev 0A
Date: Tuesday, February 09, 2010	Sheet 23	of 52

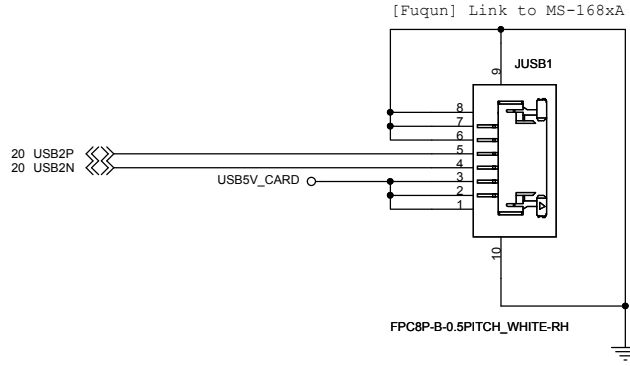
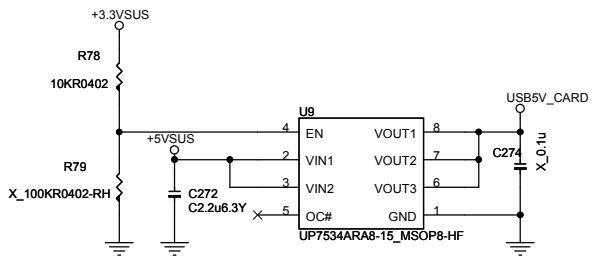
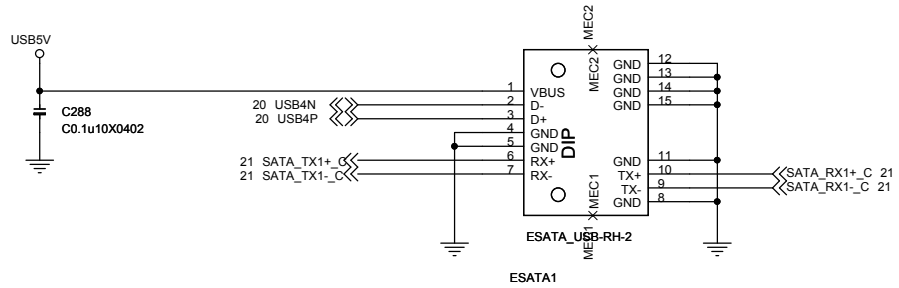
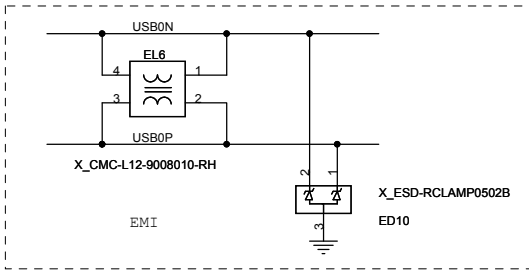
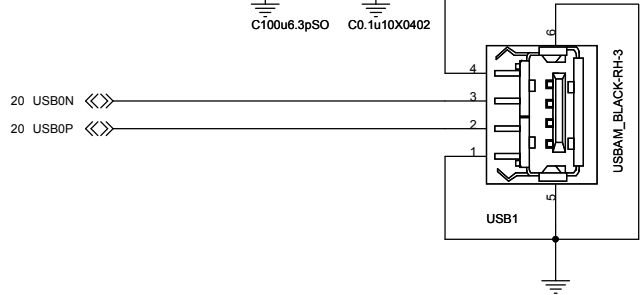
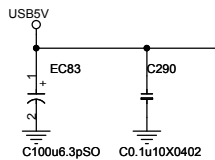
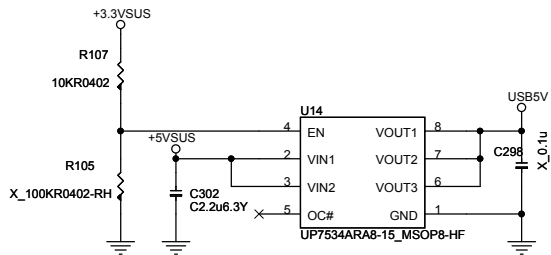


LVDS



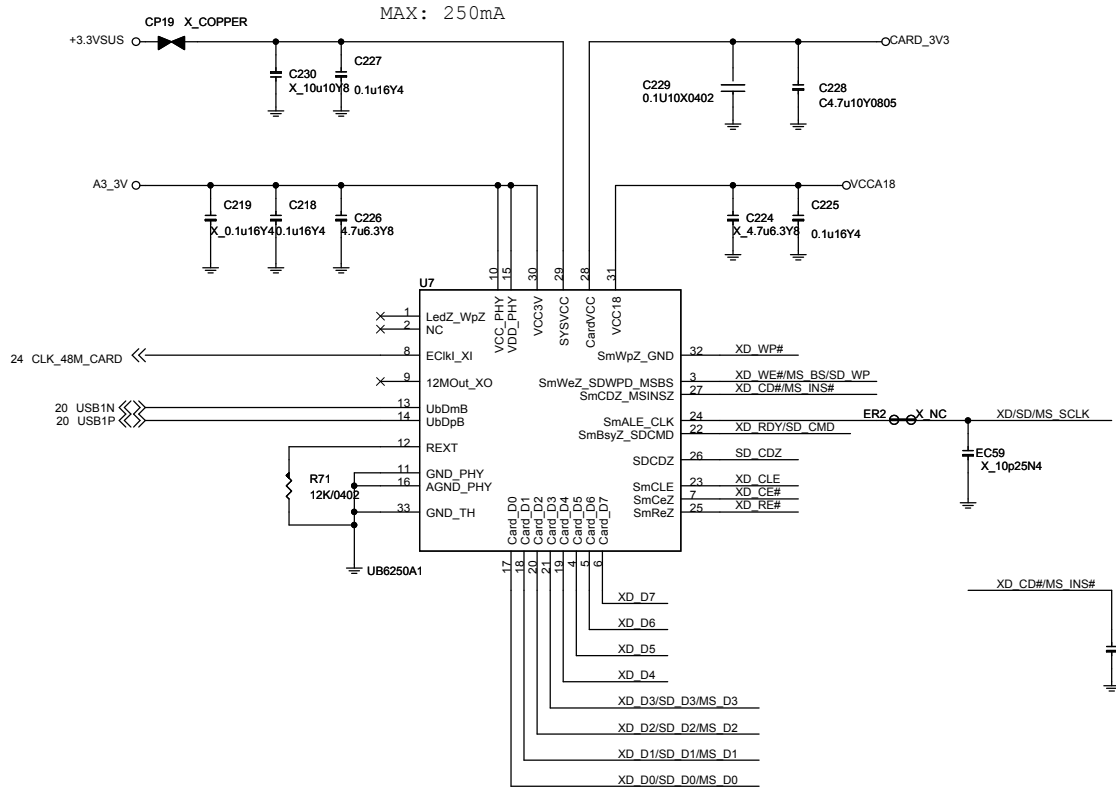


MICRO-STAR INT'L CO.,LTD		
MS-168x		
Size B	Document Description HDMI	Rev 0A
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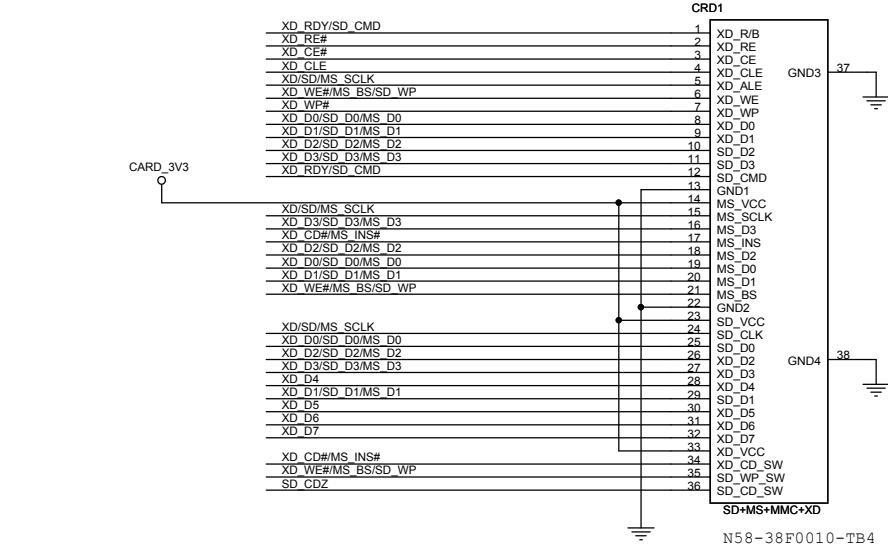


MICRO-STAR INT'L CO.,LTD		
MS-168x		
Size Custom	Document Description USB and ESATA	Rev 0A
Date: Friday, February 05, 2010	Sheet 28 of 50	1

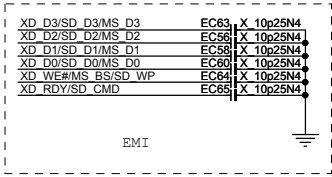
Card Reader controller




Flash Card Socket



ENE UB6250 USB20 Flash Card Reader Controller						
Pins for SD, MMC, MS, and xD memory cards						
Name	No	I/O	XD	SD	MMC	MS
xDCEZ	7	O	xD card EN			
xDCE	23	O	xD CMD latch EN			
xDAlE	24	O	xD ADDR latch EN			
xDBSyZ	22	B	xD Ready/busy	SD clock	MMC clock	MS serial clock
xDData0	17	B	xD D0	SD D0	MMC D0	MS D0
xDData1	18	B	xD D1	SD D1	MMC D1	MS D1
xDData2	20	B	xD D2	SD D2	MMC D2	MS D2
xDData3	21	B	xD D3	SD D3	MMC D3	MS D3
xDData4	19	B	xD D4		MMC D4	MS D4
xDData5	4	B	xD D5		MMC D5	MS D5
xDData6	5	B	xD D6		MMC D6	MS D6
xDData7	6	B	xD D7		MMC D7	MS D7
xDWeZ	3	B	xD W EN	SD WP		MS Busy
xDReZ	25	O	xD R EN			
xDWpZ	32	O	xD WP			
SDCDZ	26	I		SD CD	MMC CD	
xDCdZ	27	I	xD CD			MS CD





MICRO-STAR INT'L CO.,LTD

MS-168x

Size Custom

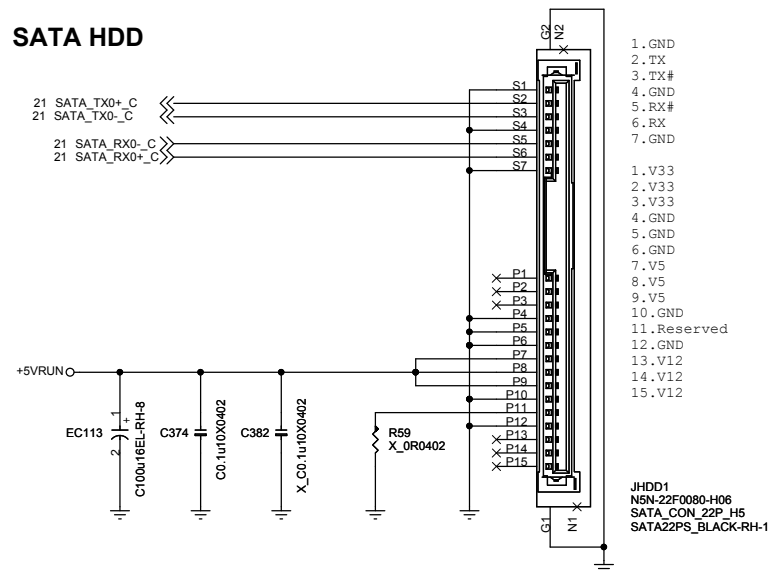
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Rev 0A

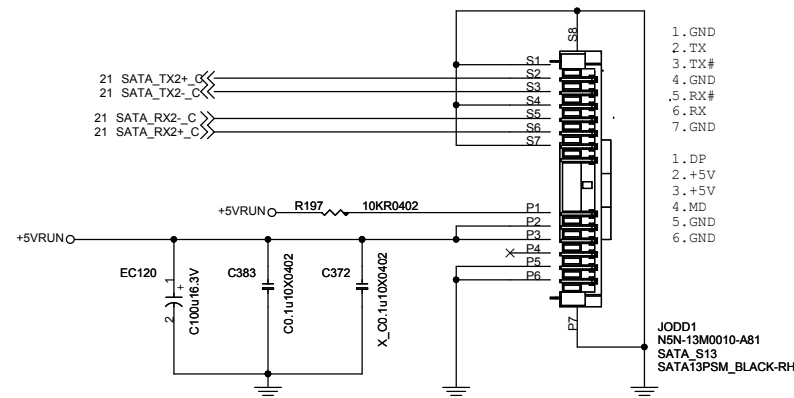
Date: Friday, February 05, 2010

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SATA HDD

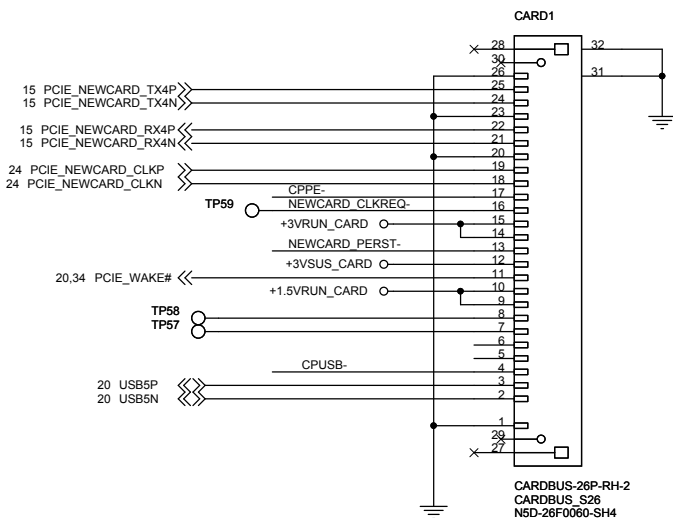
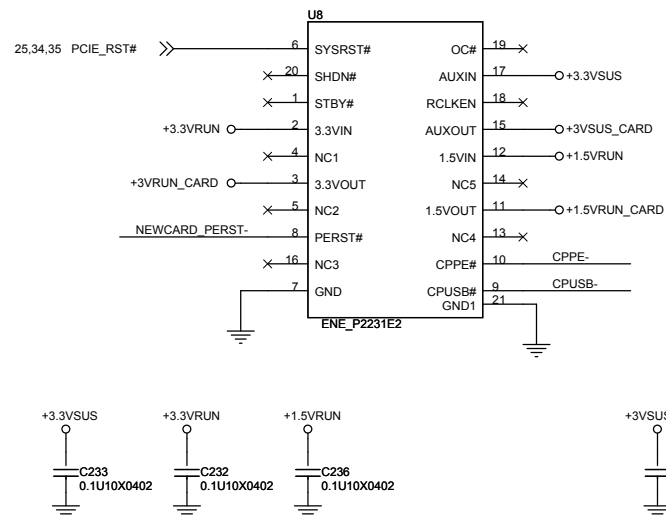


SATA ODD



NEW CARD

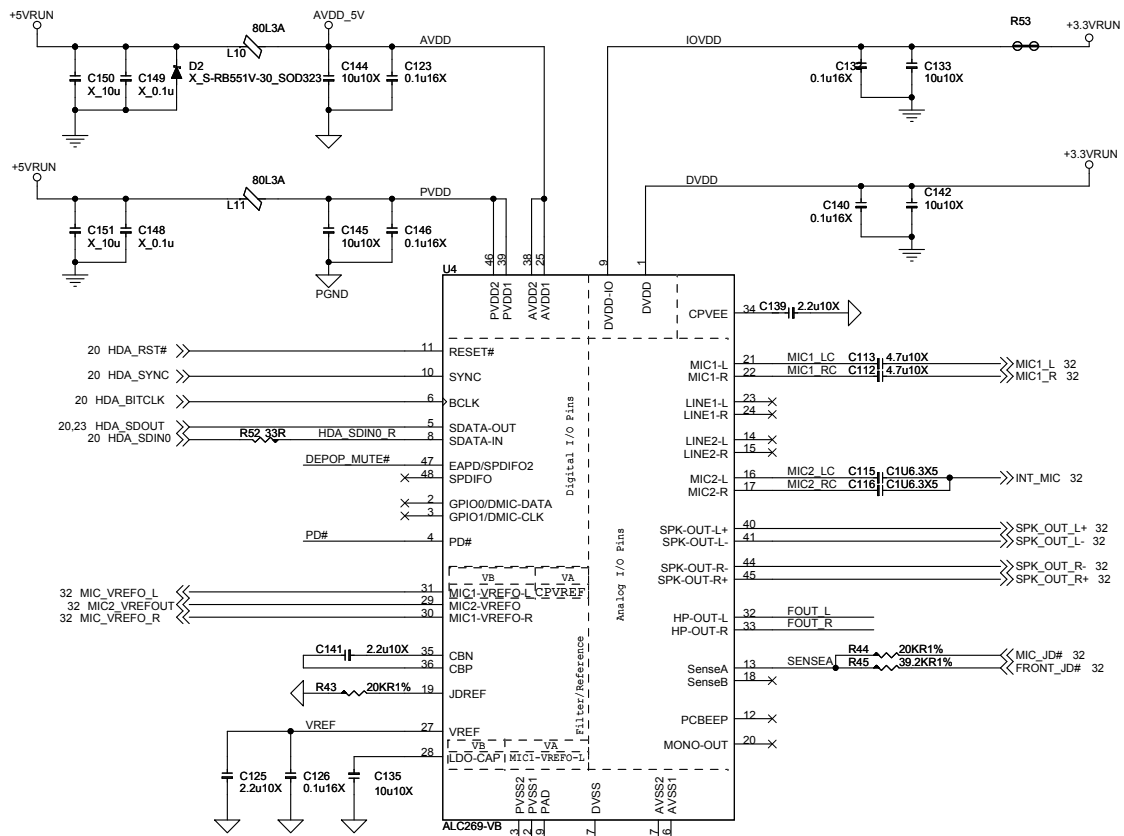
[CheckList] PCIE_RST# and GPIO_RST#-->PCIE device



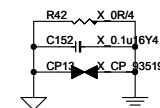
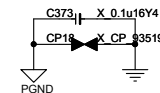
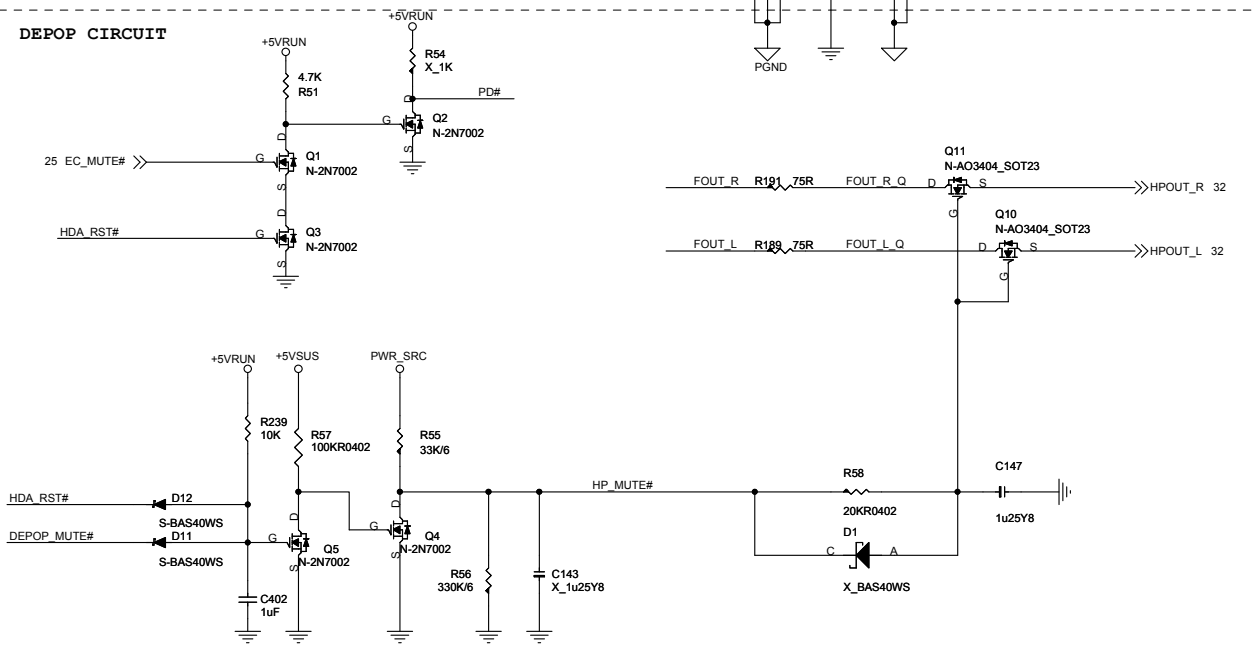
MICRO-STAR INT'L CO.,LTD

MS-168x

Size	Document Description	Rev
Custom	HDD/ODD/NEW CARD	0A
Date:	Monday, February 08, 2010	Sheet 30 of 52



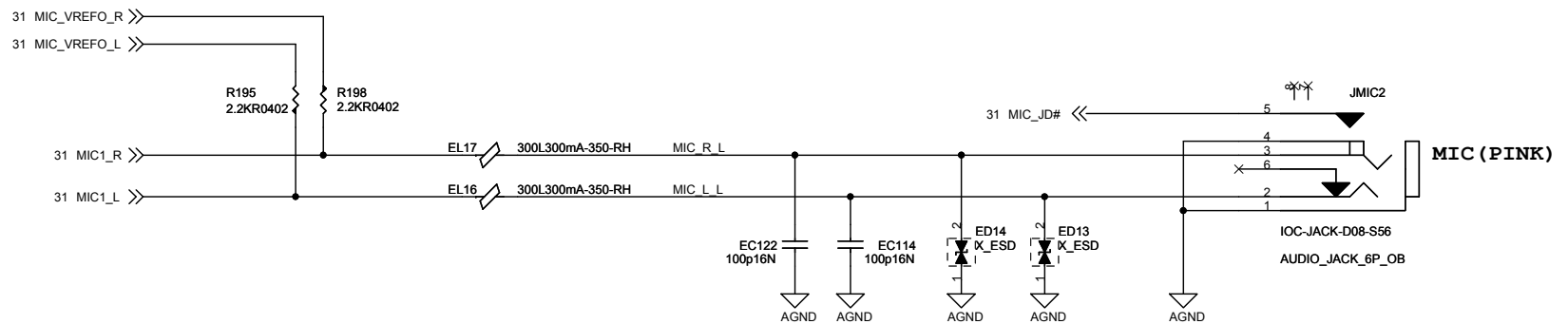
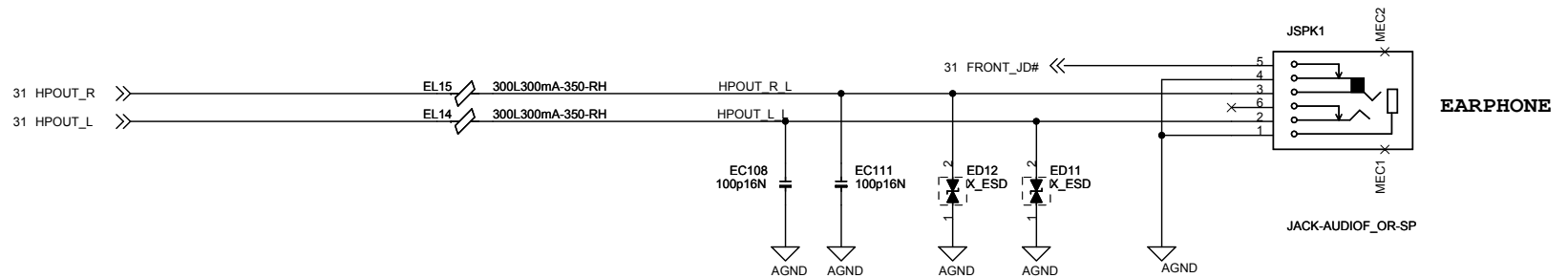
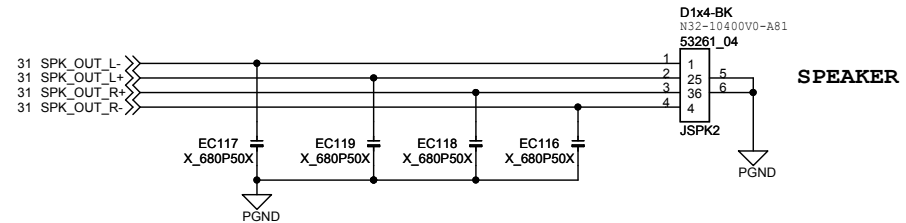
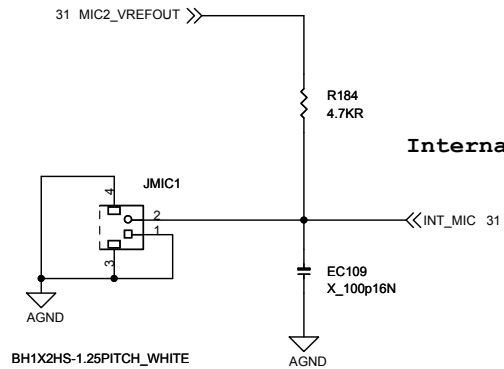
DEPOP CIRCUIT



MICRO-STAR INT'L CO.,LTD

MS-168x

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Size
B

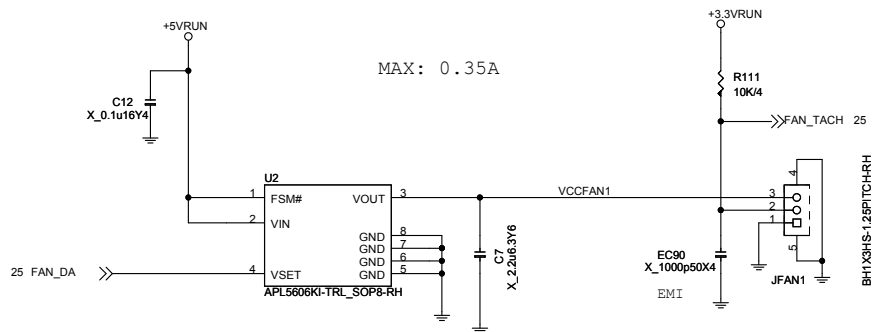
Document Description
SPK / HP / MIC

Rev
0A

Date: Friday, February 05, 2010

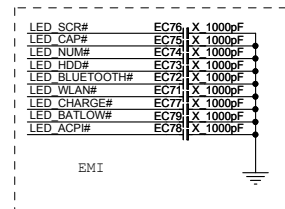
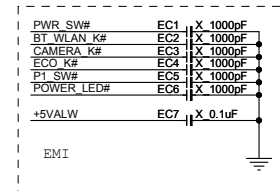
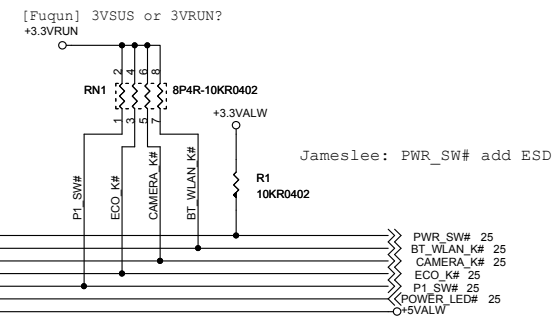
Sheet 32 of 52

FAN

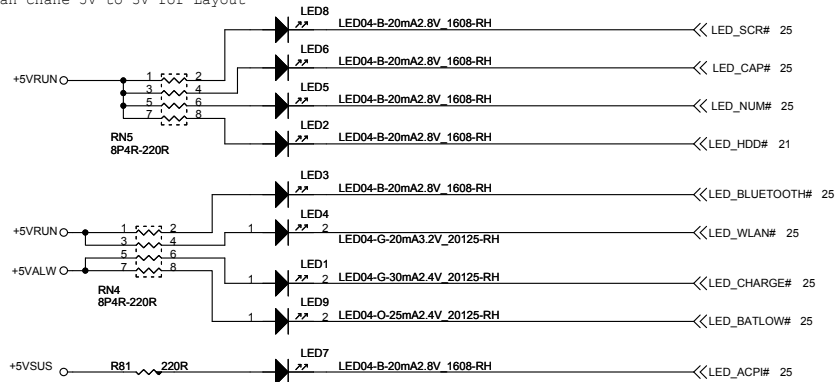


[Fuqun] P/N follow 1684 or 1688?

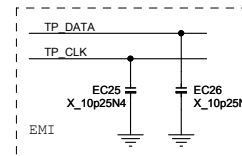
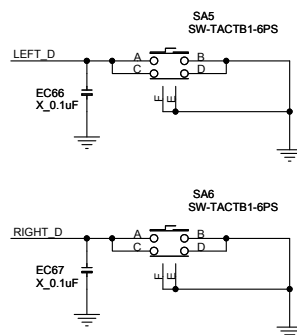
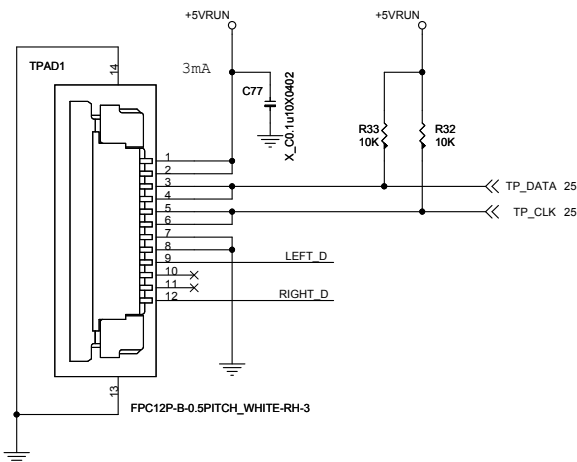
[Fuqun] Link to MS-168x



[Fuqun] Can chane 5V to 3V for Layout



TOUCH PAD

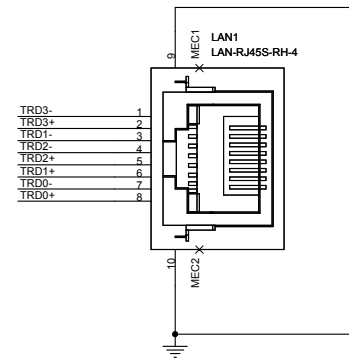
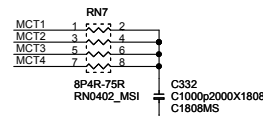
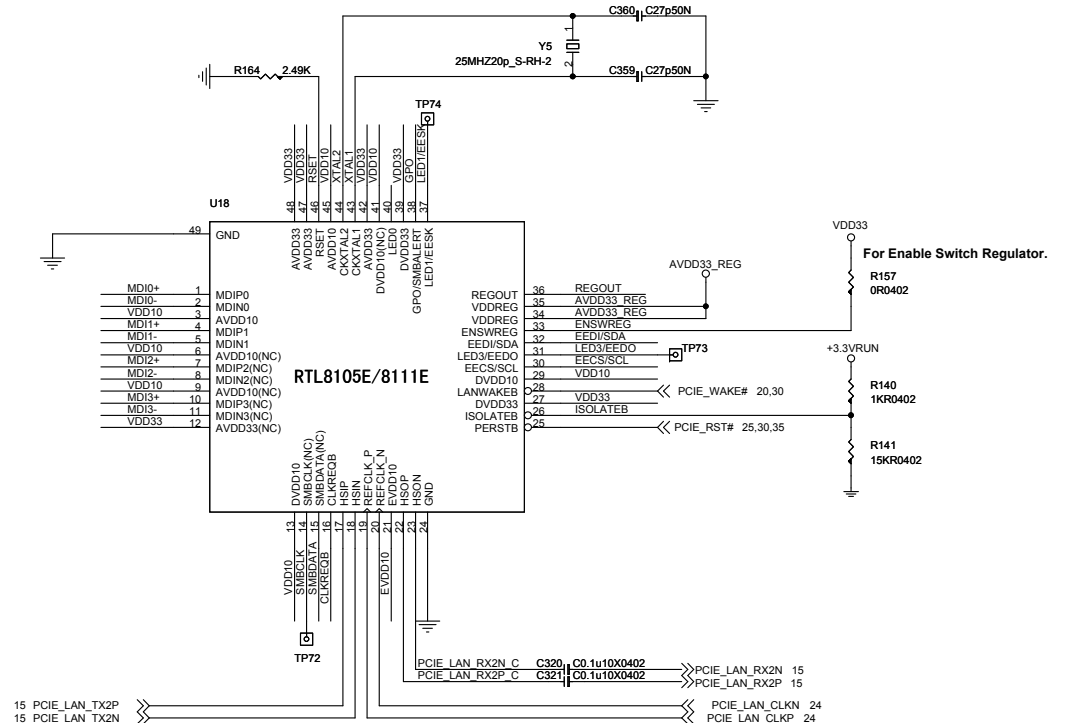
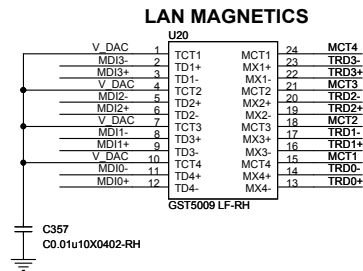
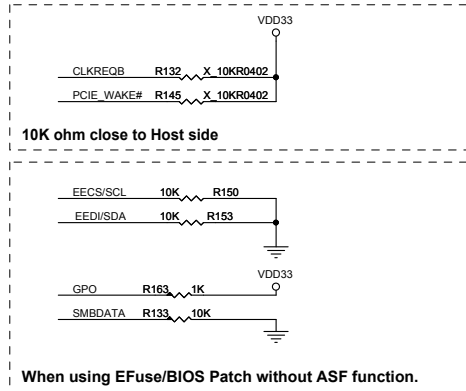
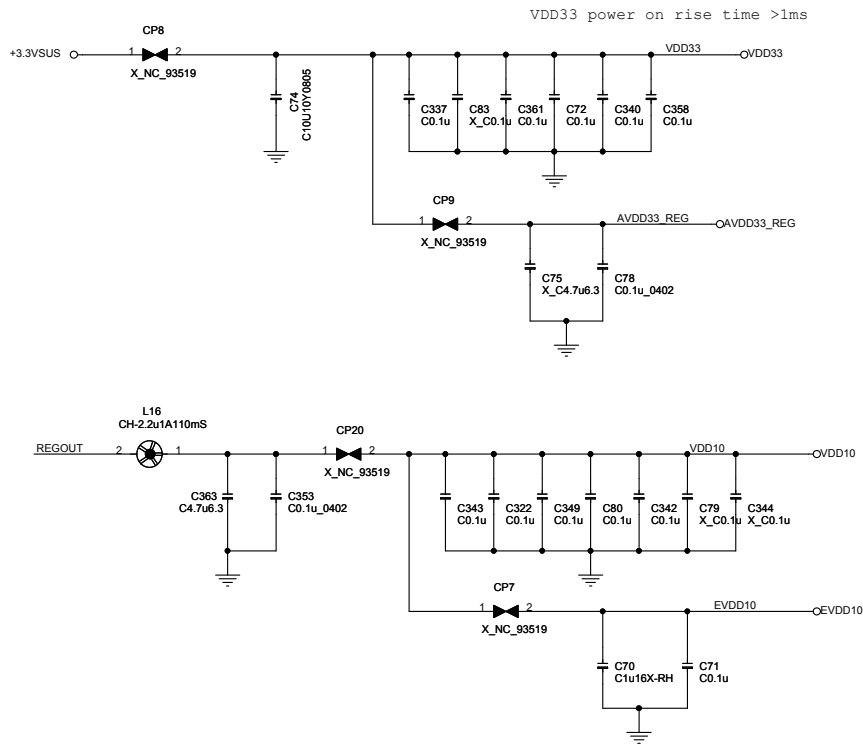


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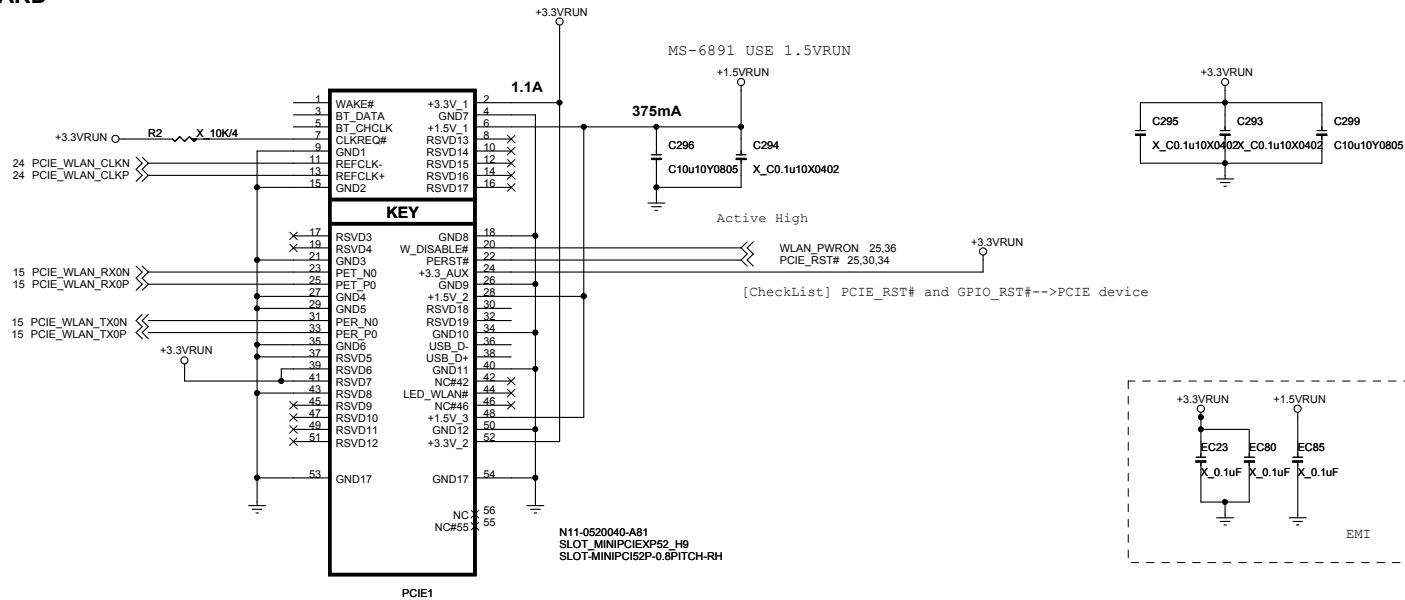
MS-168x

Size Custom Document Description FAN/LED/TP Rev 0A

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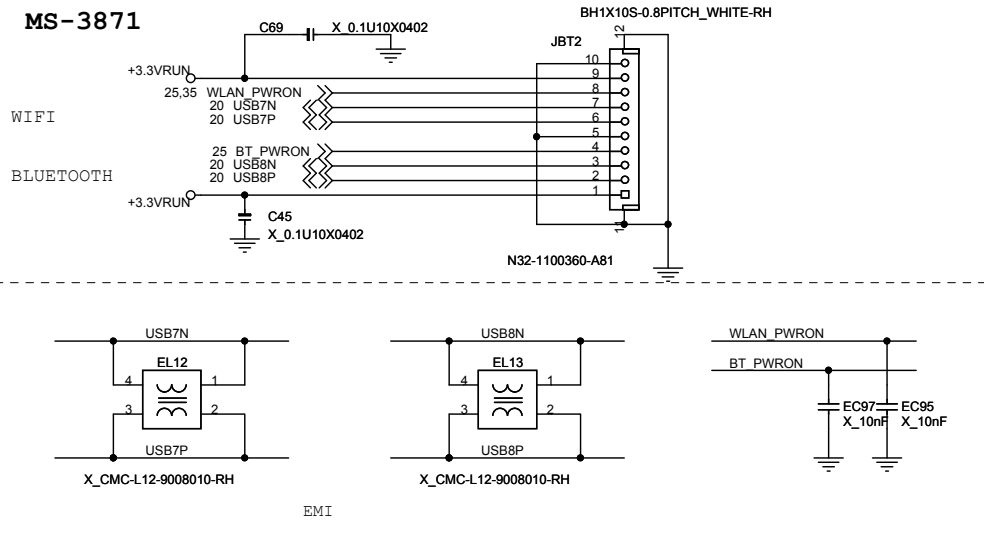


WLAN CARD



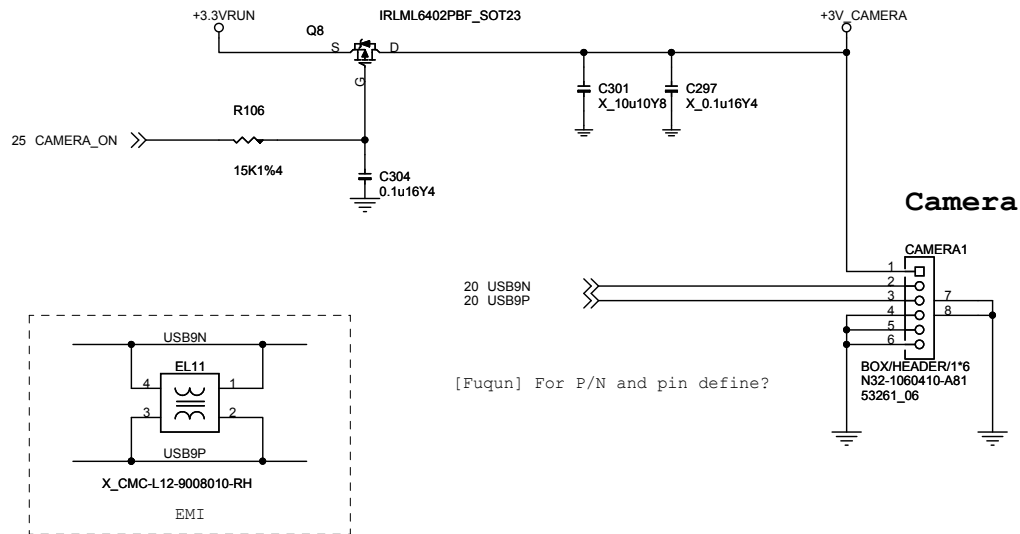
BLUETOOTH

MS-3871



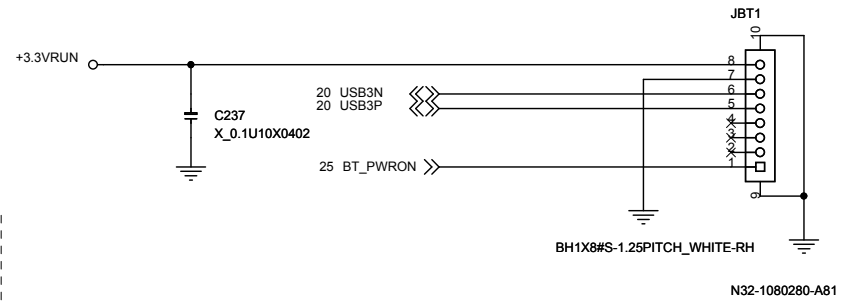
CAMERA

MAX: 130mA

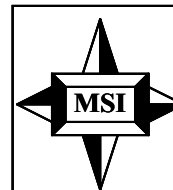
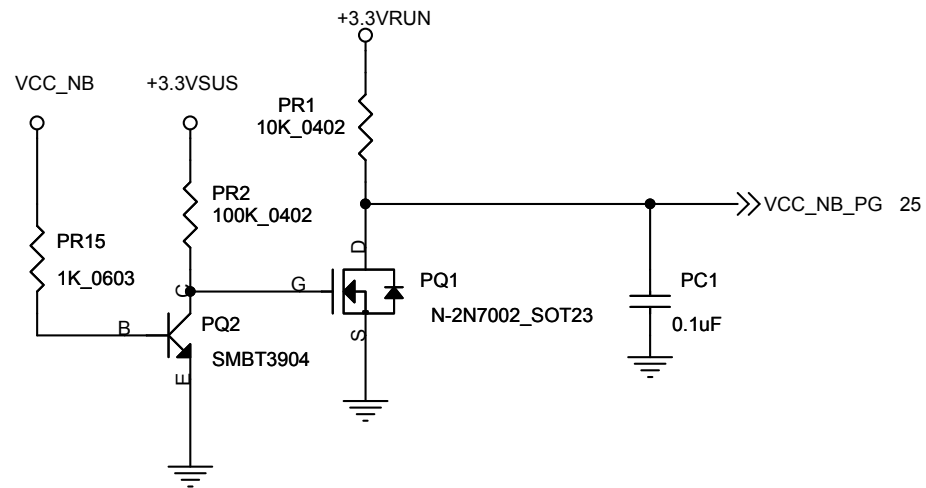


BLUETOOTH

MS-3801



MICRO-STAR INT'L CO.,LTD			
MS-168x			
Size B	Document Description CAMERA/BT		Rev 0A
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MICRO-STAR INT'L CO.,LTD

MS-168x

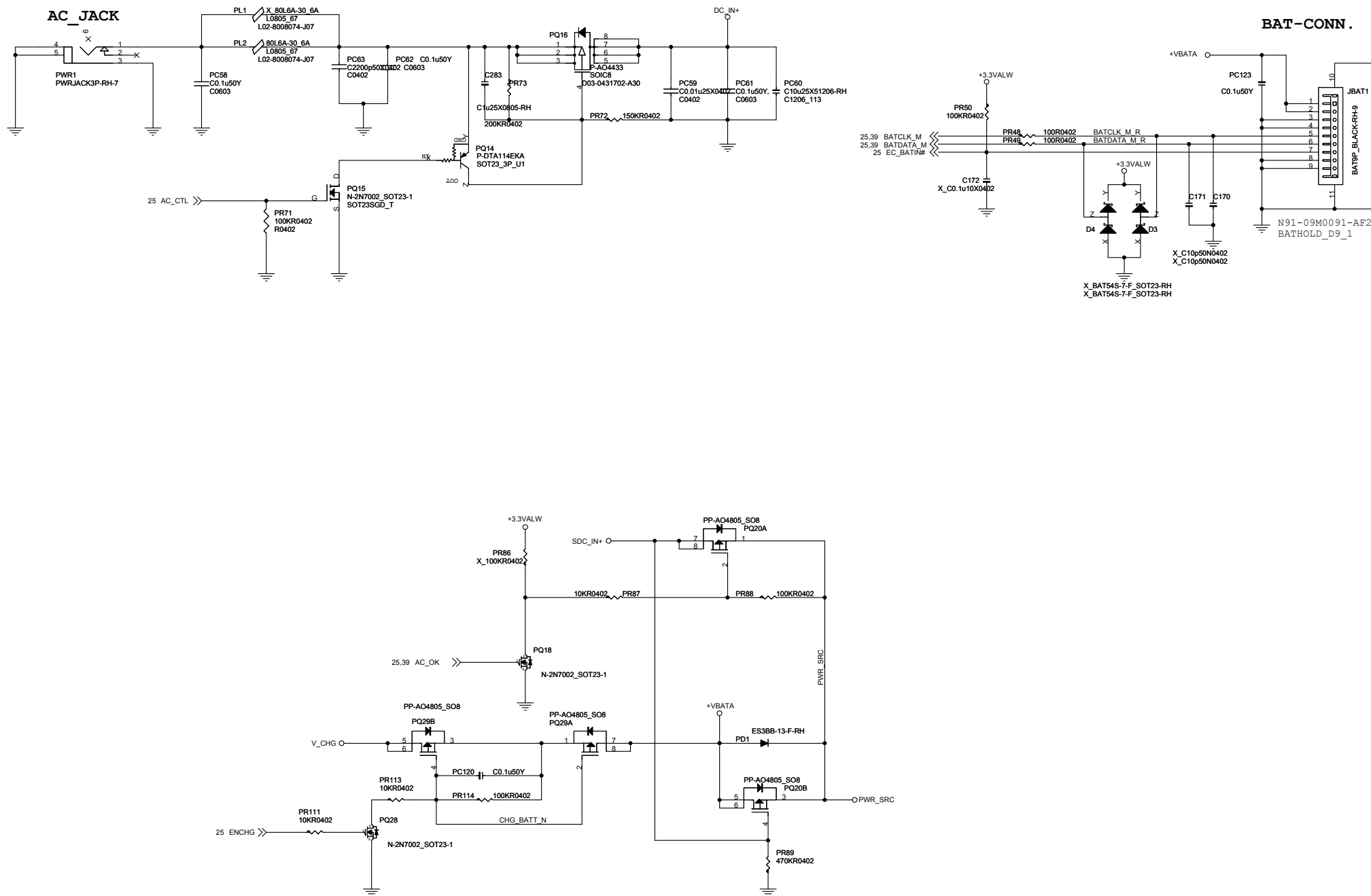
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Document Description
POWER LOGIC

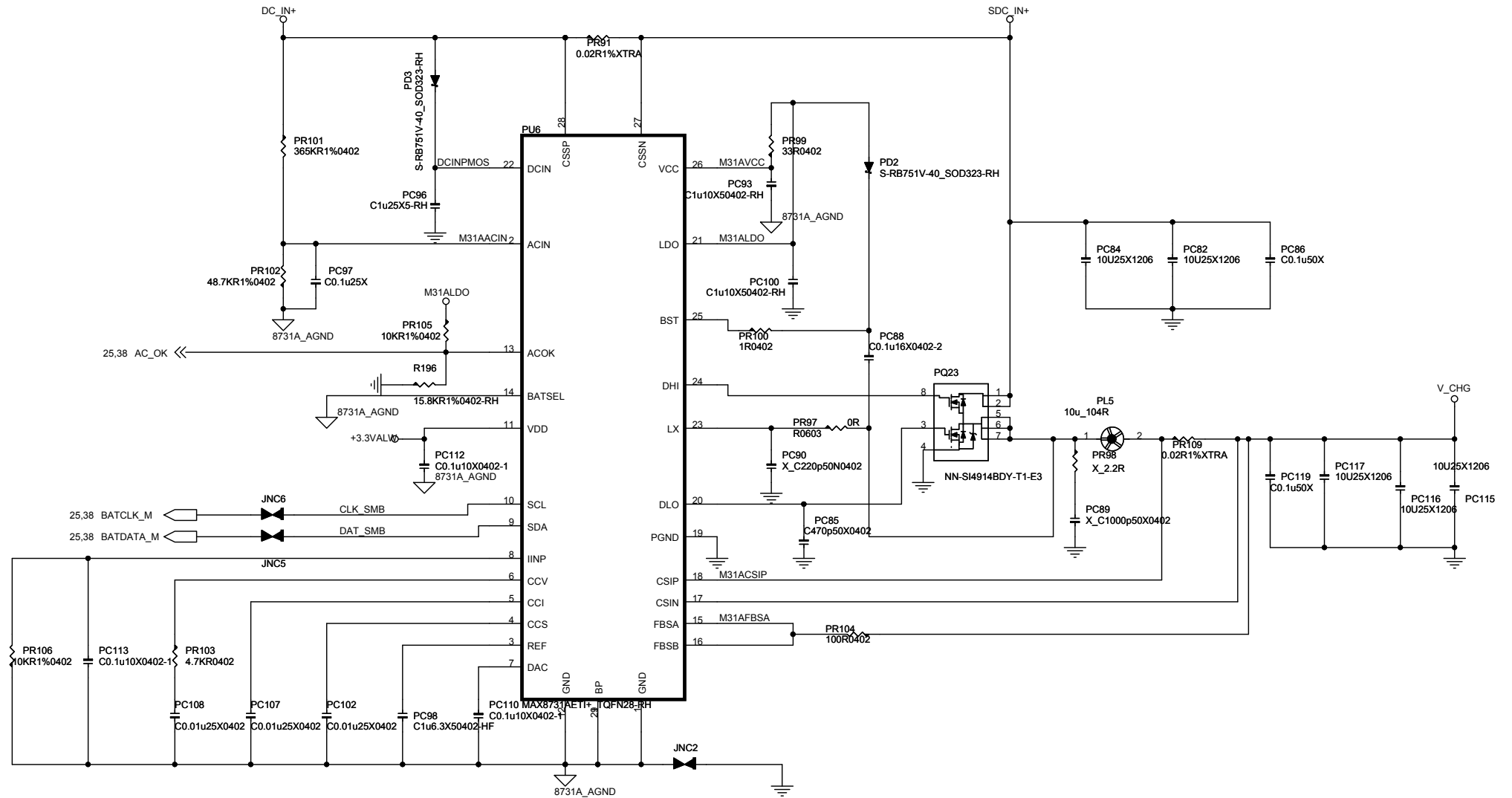
Rev
0A

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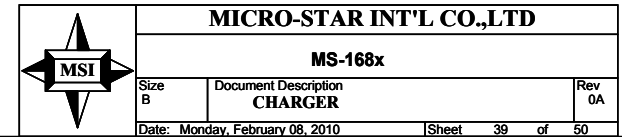


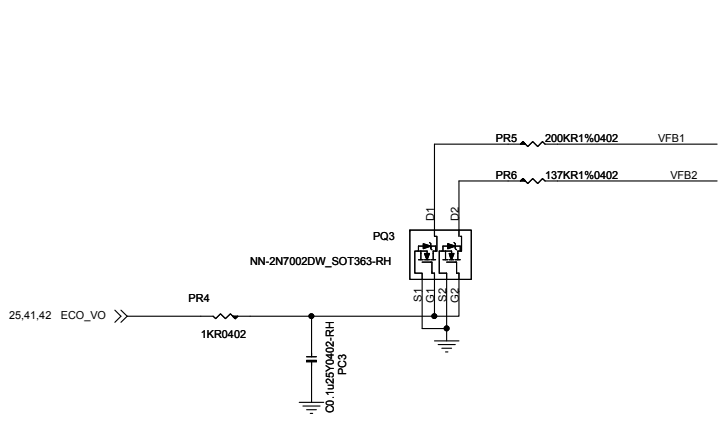
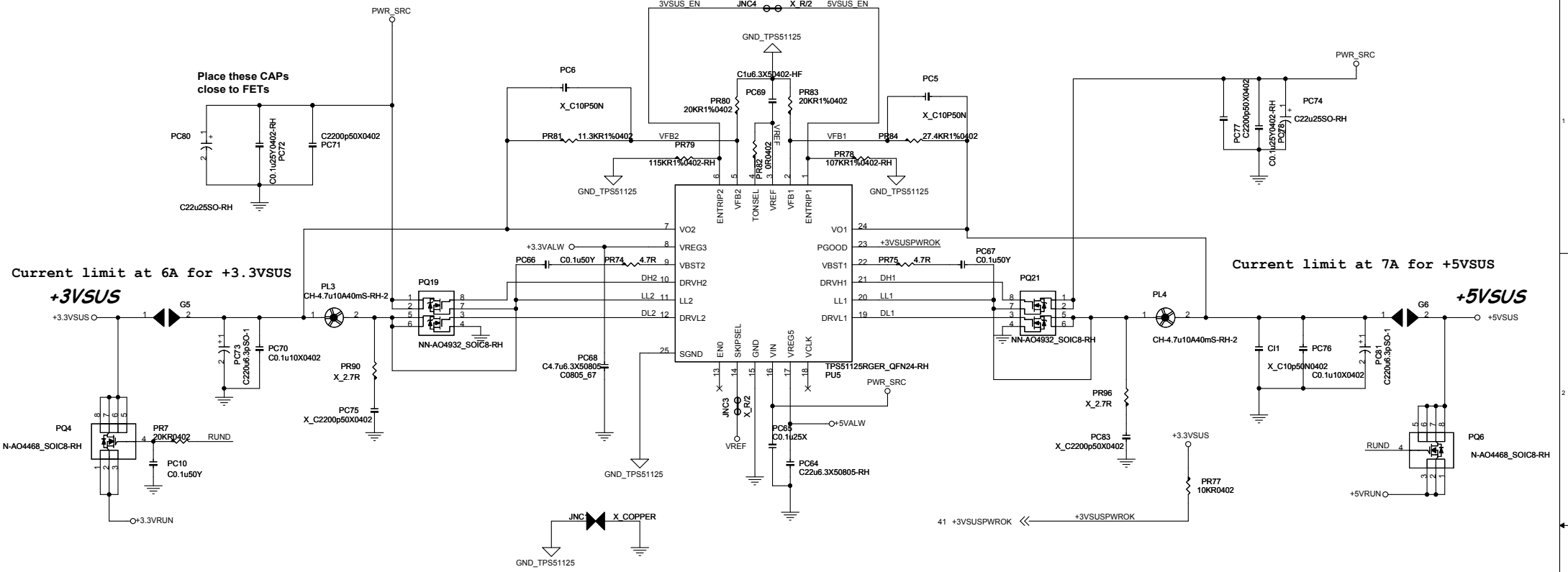
Adapter input voltage set 19 Voltage



IINP :

1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
2. $V_{IINP} = IINP_{UT} \times RS1 \times 3mA/V \times PR25$



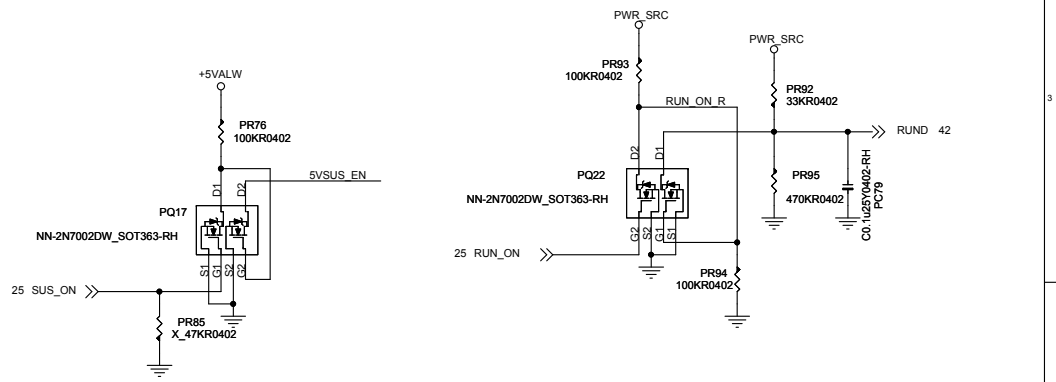


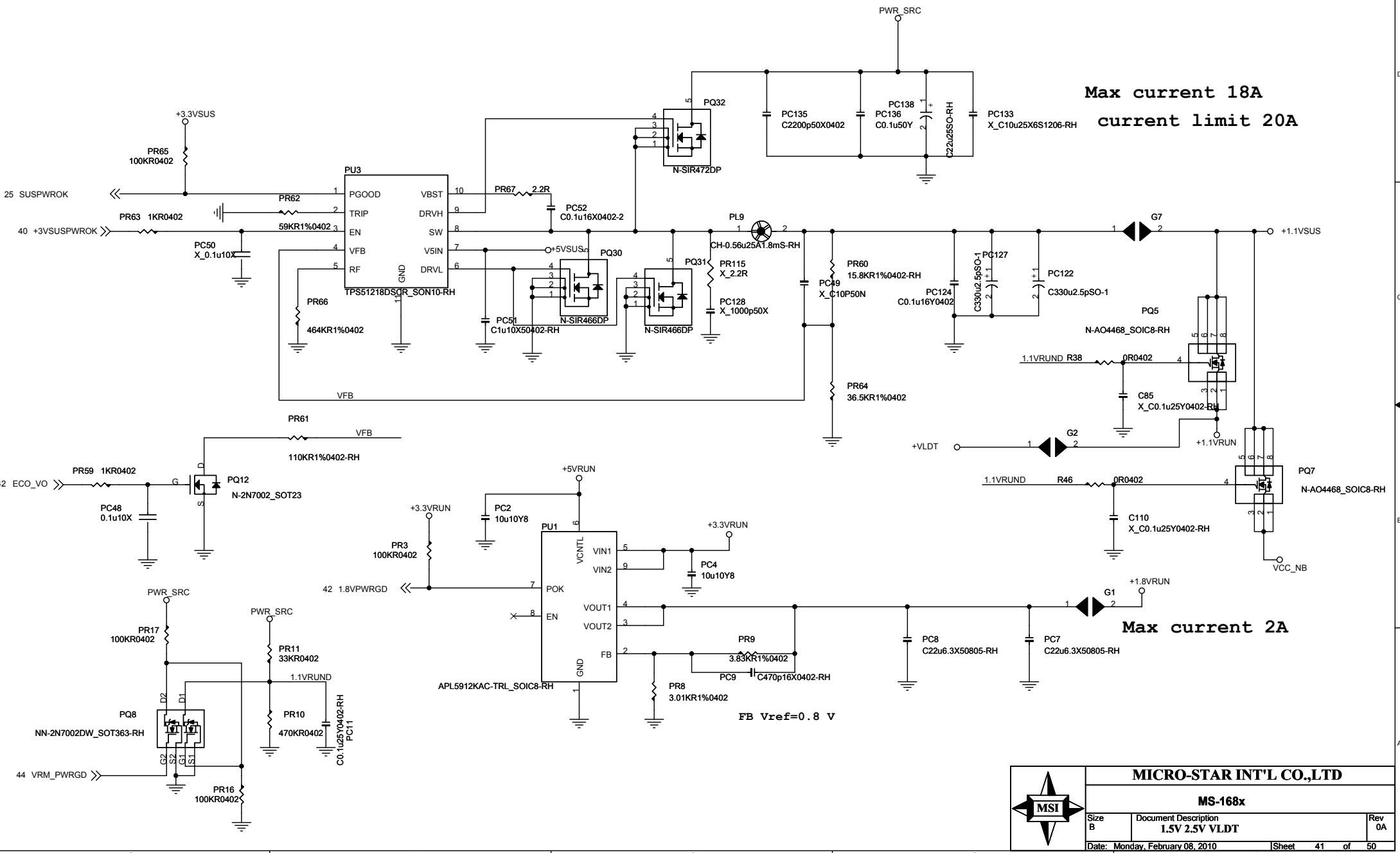
+3VSUS Voltage TABLE

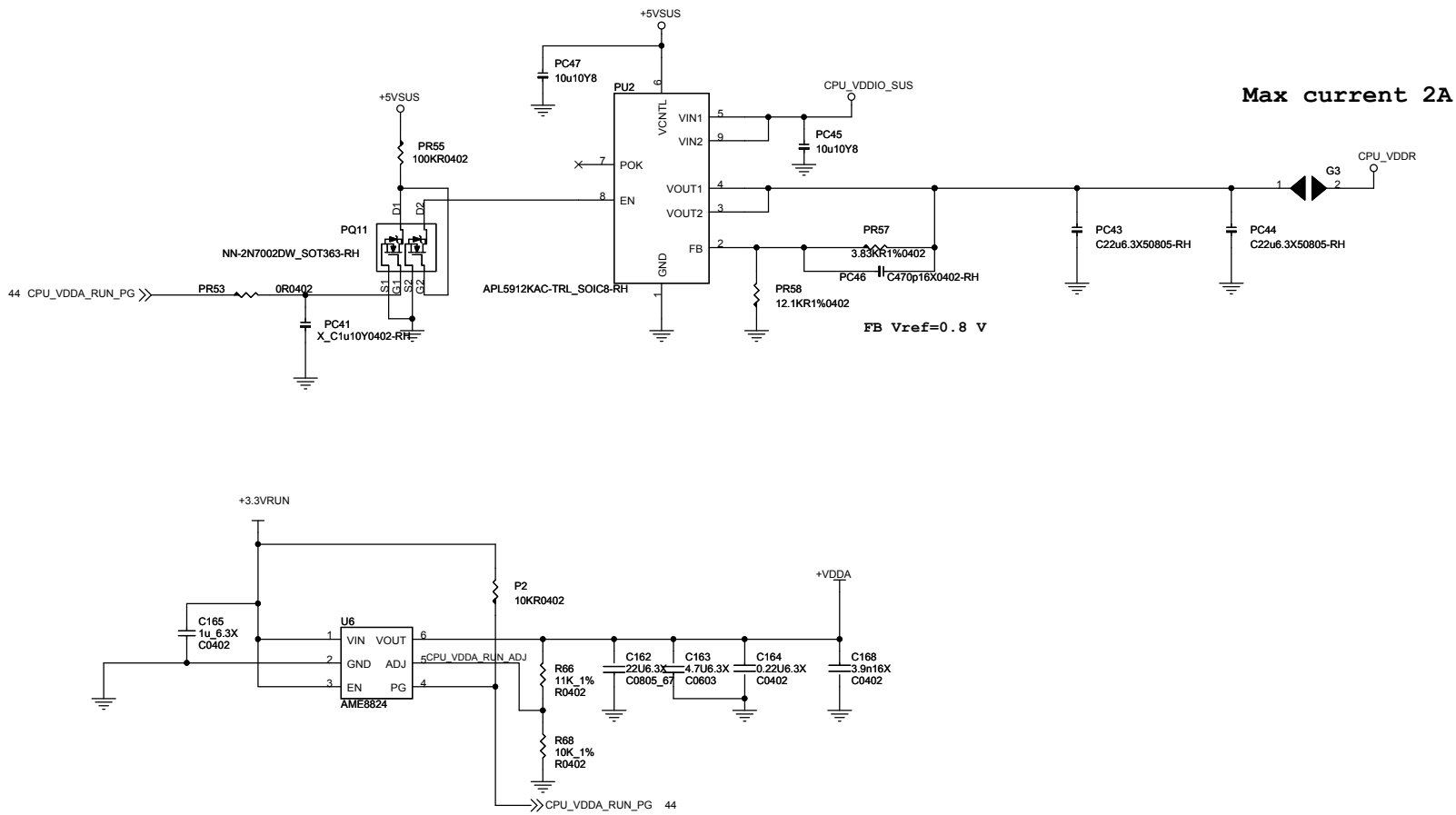
ECO_VO	Voltage
HIGH	3.3V(default)
LOW	3.15V

+5VSUS Voltage TABLE

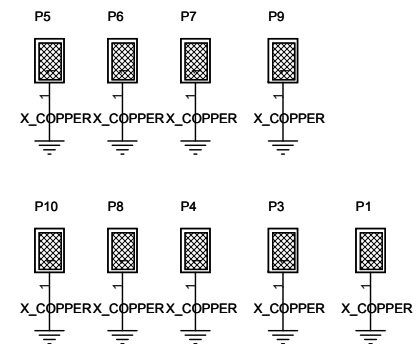
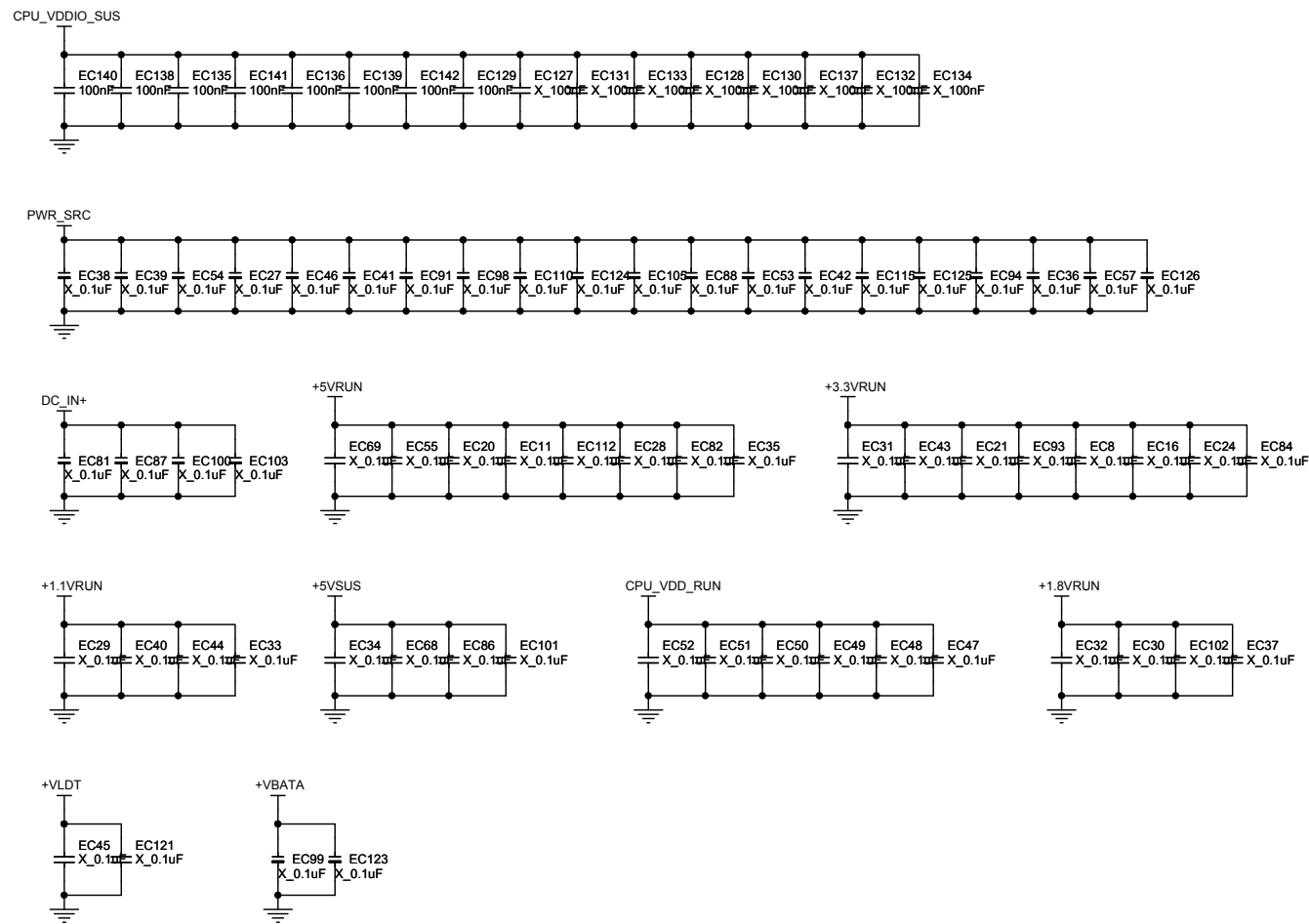
ECO_VO	Voltage
HIGH	5V(default)
LOW	4.8V







MICRO-STAR INT'L CO.,LTD			
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MS-168x

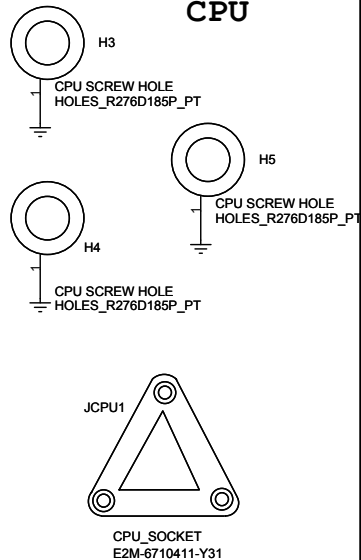
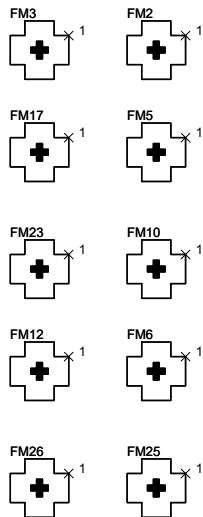
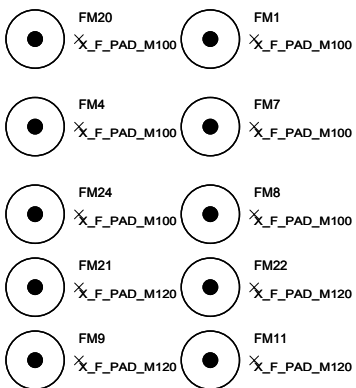
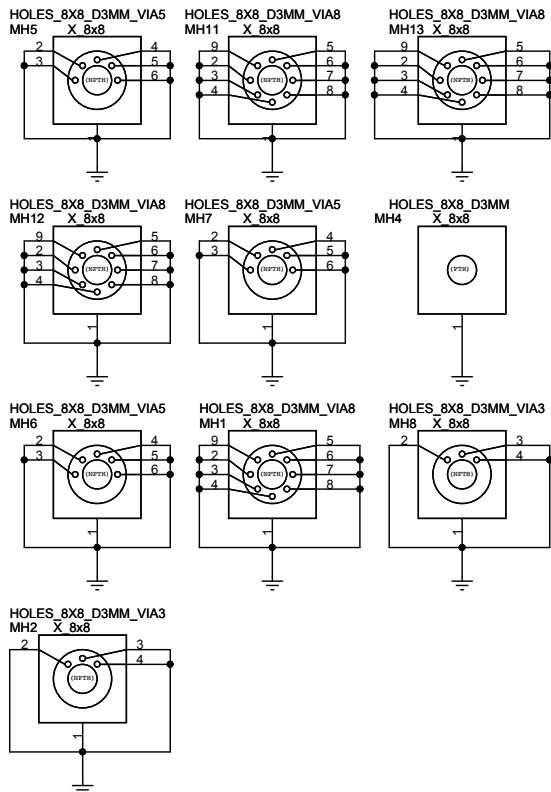
Size
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Document Description
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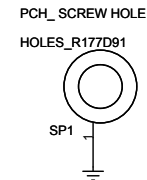
Rev
0A

Date: Friday, February 05, 2010

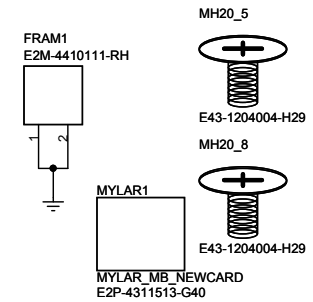
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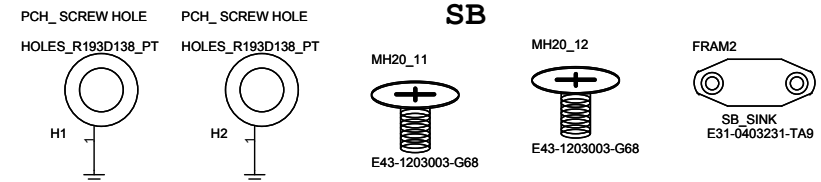
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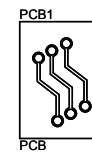
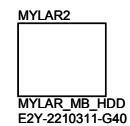
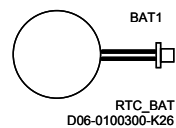
NEW CARD



SB



FOR HDD

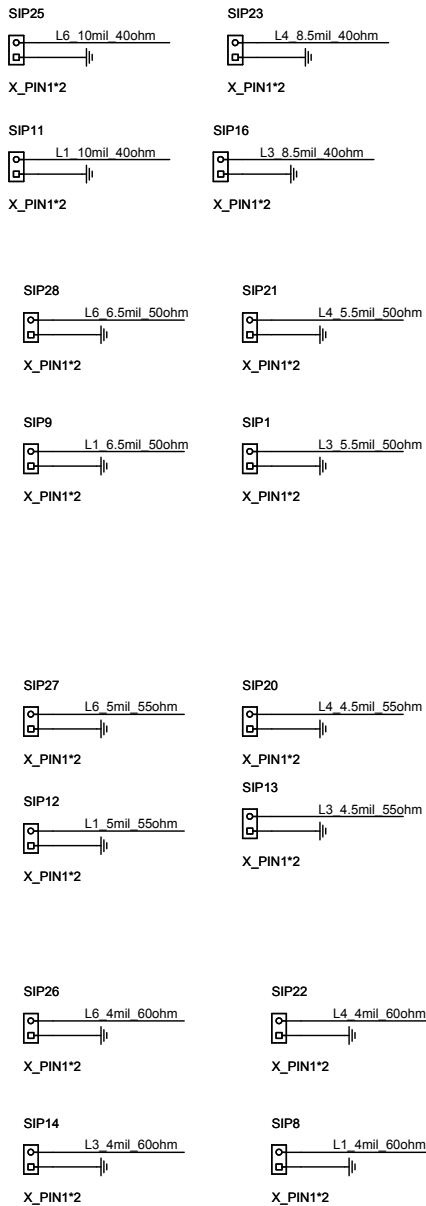


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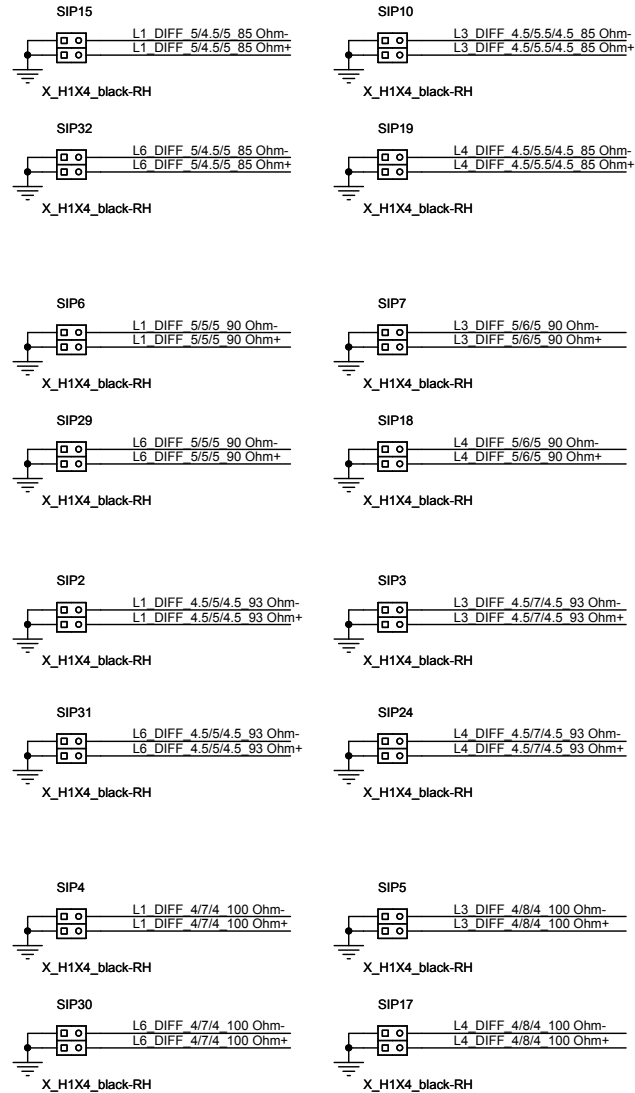
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Single ended



Differential signal



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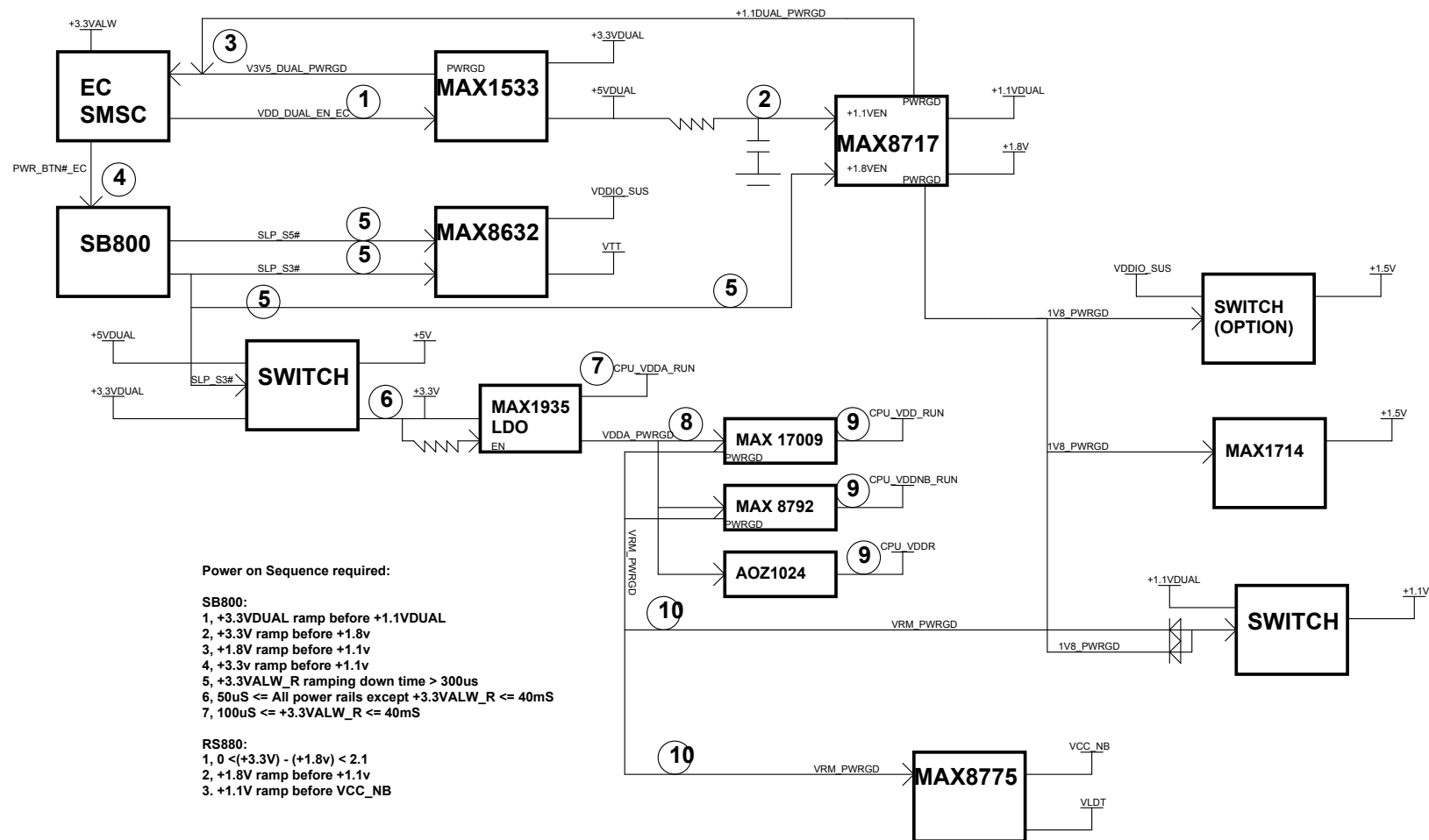
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Power on Sequence required:

SB800:

- 1, $+3.3VDUAL$ ramp before $+1.1VDUAL$
- 2, $+3.3V$ ramp before $+1.8v$
- 3, $+1.8V$ ramp before $+1.1v$
- 4, $+3.3v$ ramp before $+1.1v$
- 5, $+3.3VALW_R$ ramping down time $> 300us$
- 6, $50uS \leq$ All power rails except $+3.3VALW_R \leq 40mS$
- 7, $100uS \leq +3.3VALW_R \leq 40mS$

RS880:

- 1, $0 < (+3.3V) - (+1.8v) < 2.1$
- 2, $+1.8V$ ramp before $+1.1v$
- 3, $+1.1V$ ramp before VCC_NB

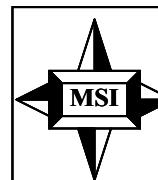
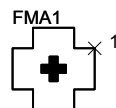
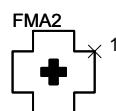
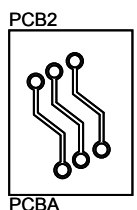
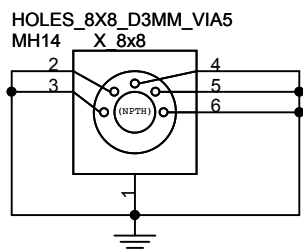
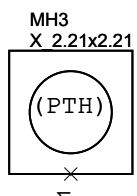
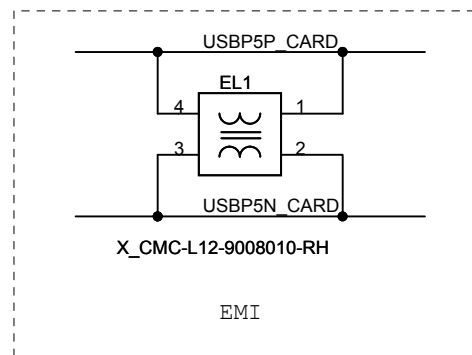
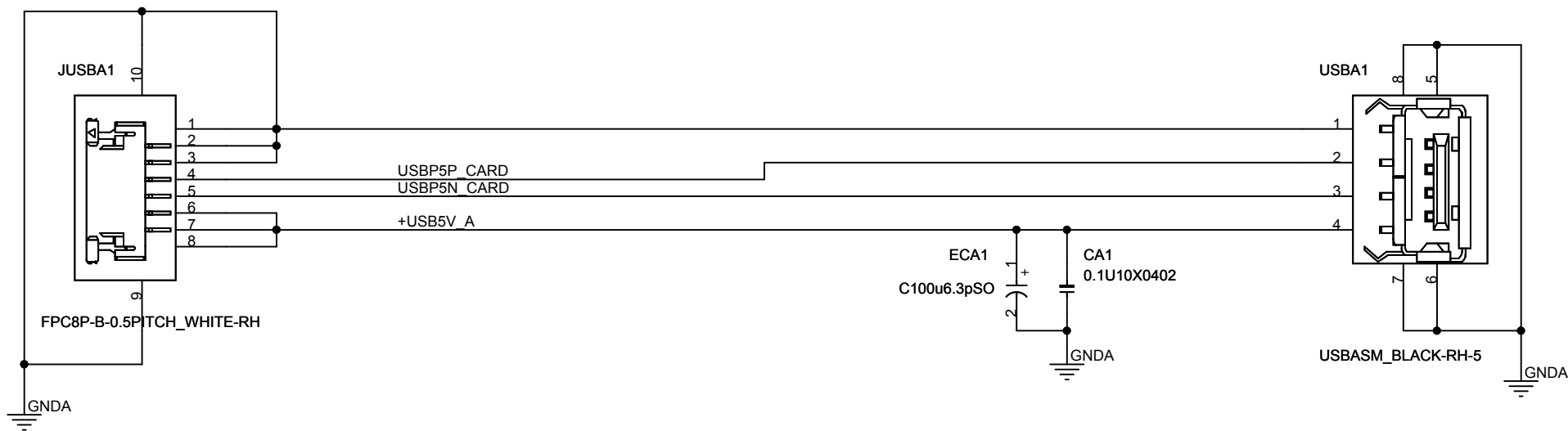


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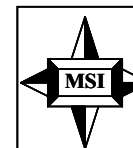
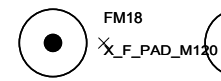
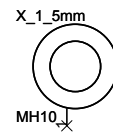
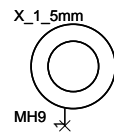
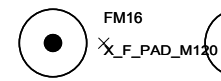
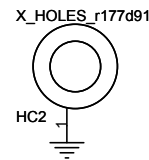
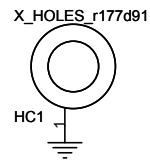
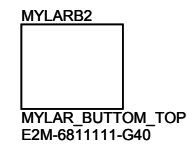
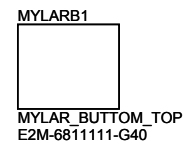
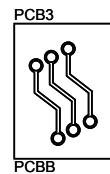
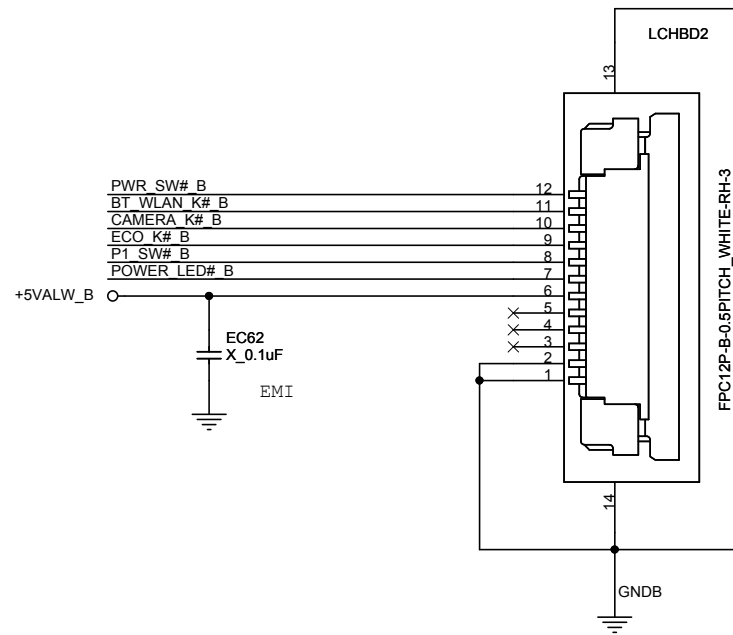
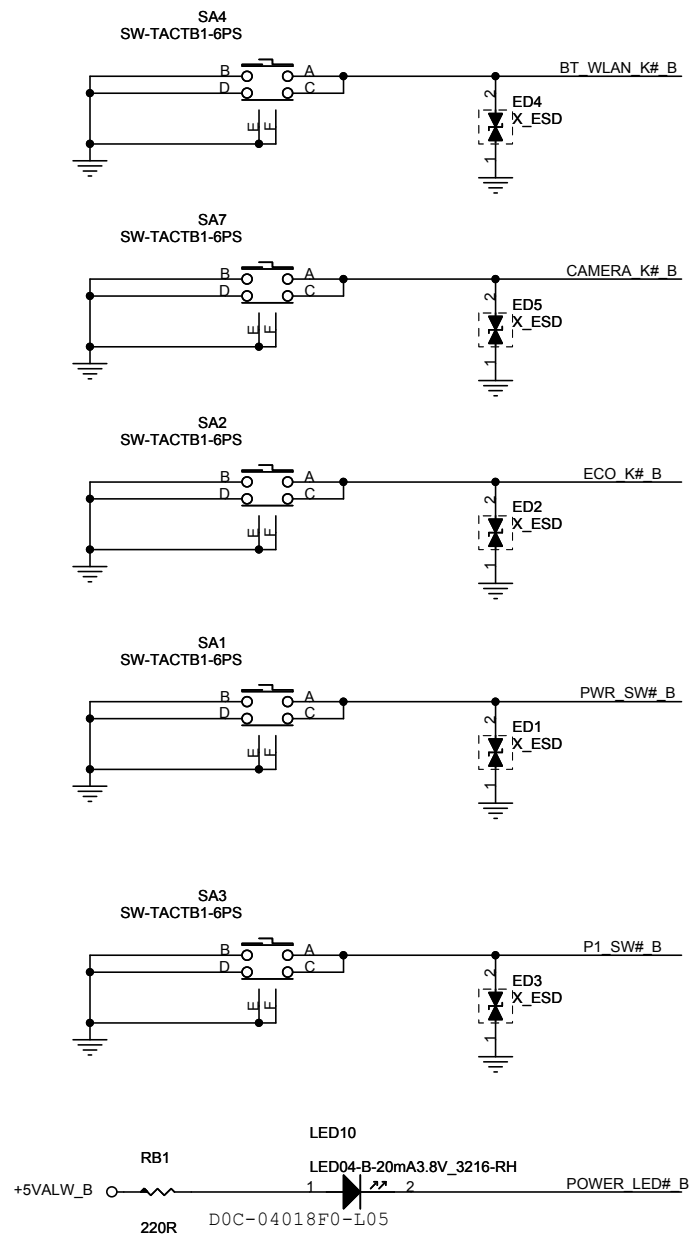
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